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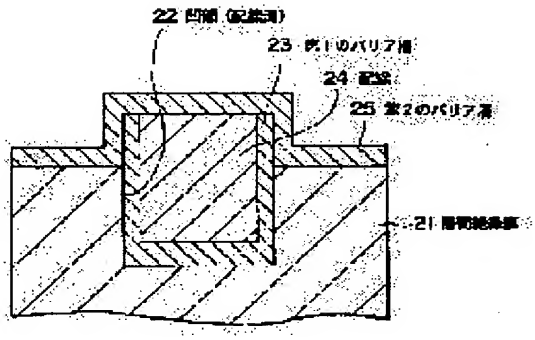
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent migration of copper in a copper wiring from an interface between a barrier metal layer and a nitride layer to an interlayer insulating film and thus to prevent the occurrence of a leak current and a short circuit between neighboring wirings, by simply covering the upper surface of the copper wiring formed in a wiring trench via a barrier metal layer with a nitride film.
SOLUTION: A semiconductor device having a wiring 24 formed in a recessed portion (wiring trench) 22 formed in an interlayer insulating film 21 has a first barrier layer 23 covering the wiring 24 from under the wiring 24, and a second barrier layer 25 covering the wiring 24 from over the wiring 24, wherein the first barrier layer 23 overlaps the second barrier layer 25.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device characterized by having the 1st barrier layer which covers the wiring concerned from the lower part side of said wiring, and the 2nd barrier layer which covers the wiring concerned from the upper part side of said wiring, and for said 1st barrier layer and said 2nd barrier layers overlapping, and covering said wiring in the semiconductor device which equipped with wiring the interior of the crevice formed in the interlayer insulation film.
[Claim 2] The overlapping parts of said 1st barrier layer and said 2nd barrier layer are semiconductor devices according to claim 1 characterized by what is prepared in the flank of said wiring.
[Claim 3] The overlapping parts of said 1st barrier layer and said 2nd barrier layer are semiconductor devices according to claim 1 characterized by being prepared in the top section of said wiring.
[Claim 4] Said crevice is a semiconductor device according to claim 1 characterized by consisting of a slot, a connection hole, or a connection hole formed in the pars basilaris ossis occipitalis of a slot and this slot.
[Claim 5] The process which forms wiring in the interior of said crevice by embedding a conductor while forming the 1st barrier layer in the inside of said crevice after forming a crevice in an insulator layer, The process which said insulator layer around said wiring is removed [process], and makes said wiring and said 1st barrier layer project from said insulator layer front face, The manufacture approach of the semiconductor device characterized by having the process which overlaps said 1st barrier layer by the flank of said wiring with a wrap in the upper part side of said wiring, and forms the barrier layer of a wrap 2nd for said wiring with said 1st barrier layer.
[Claim 6] The manufacture approach of the semiconductor device according to claim 5 characterized by performing even the process which forms said 2nd barrier layer from the process which removes said insulator layer around said wiring by the non-oxidizing atmosphere.
[Claim 7] Said crevice is the manufacture approach of the semiconductor device according to claim 5 characterized by being formed with a slot, a connection hole, or the connection hole formed in the pars basilaris ossis occipitalis of a slot and this slot.
[Claim 8] The process which forms wiring in the interior of said crevice by embedding a conductor while forming the 1st barrier layer in the inside of said crevice after forming a crevice in an insulator layer, The manufacture approach of the semiconductor device characterized by having the process which removes said insulator layer near the top section of said 1st barrier layer, and forms a slot, and the process which forms the 2nd barrier layer in the condition of embedding said slot for the upper part side of said wiring with a wrap.
[Claim 9] The manufacture approach of the semiconductor device according to claim 8 characterized by performing even the process which forms said 2nd barrier layer from the process which removes said insulator layer around said wiring by the non-oxidizing atmosphere.
[Claim 10] Said crevice is the manufacture approach of the semiconductor device according to claim 8 characterized by being formed with a slot, a connection hole, or the connection hole formed in the pars basilaris ossis occipitalis of a slot and this slot.

[Claim 11] The process which forms wiring in the interior of said crevice by embedding a conductor while forming the 1st barrier layer in the inside of said crevice after forming a crevice in an insulator layer, The process which removes the upper part of said wiring so that it may become lower than said insulator layer front face, The manufacture approach of the semiconductor device characterized by having the process which overlaps said 1st barrier layer in the top section of said wiring with a wrap in the upper part side of said wiring, and forms the barrier layer of a wrap 2nd for said wiring with said 1st barrier layer.
[Claim 12] The manufacture approach of the semiconductor device according to claim 11 characterized by performing even the process which forms said 2nd barrier layer from the process which removes the upper part of said wiring by the non-oxidizing atmosphere.
[Claim 13] Said crevice is the manufacture approach of the semiconductor device according to claim 11 characterized by being formed with a slot, a connection hole, or the connection hole formed in the pars basilaris ossis occipitalis of a slot and this slot.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which used copper or a copper alloy for the conductor, and its manufacture approach in detail about a semiconductor device and its manufacture approach.
[0002]
[Description of the Prior Art] Contraction-ization of detailed-izing of wiring and a wiring pitch is needed with detailed-izing of a semiconductor device. Moreover, the reduction in the dielectric constant of an interlayer insulation film and low resistance-ization of wiring have been needed for coincidence with the demand of low-power-izing, improvement in the speed, etc. In the logic device, since a resistance rise especially according to detailed wiring and the increment in wiring capacity lead to the fall of the working speed of a device, the multilayer interconnection using an interlayer insulation film made detailed is needed in the low dielectric constant film.
[0003] It has caused increase of the number of processes at the same time contraction-ization of detailed-izing of wiring width of face and a pitch enlarges the aspect ratio of spacing during wiring (Rhine - and tooth-space part of - tooth space), and a burden is placed on the technique which forms long and slender detailed wiring perpendicularly as a result, the technique which embeds between detailed wiring with an interlayer insulation film and it not only enlarges the aspect ratio of the wiring [itself], but it complicates a process.
[0004] It is possible for it not to be necessary to embed a connection hole (for example, beer hall) and a wiring gutter by reflow sputtering of metals (aluminum, copper, etc.) or plating at coincidence, and for forming metal wiring of a high aspect ratio by etching not to embed **** during wiring with an interlayer insulation film in the DAMASHIN process which grinds a surface metal by chemical mechanical polishing (it is called Following CMP), either, and to reduce the number of processes sharply. This process comes to contribute to reduction of the total manufacturing cost greatly, so that the aspect ratio of wiring becomes high and a wiring total increases.
[0005] Conventionally, in wiring of LSI, although aluminum and an aluminium alloy have been used for the electrical conducting material, in order to attain improvement in the speed and low-power-ization with improvement in the degree of integration of a semiconductor integrated circuit in recent years, a copper alloy has come to be used for an electrical conducting material. moreover, DAMASHIN embedding the wiring material which the manufacture approach of using copper for a wiring material does not make an insulator layer cover after processing a wiring material by the conventional etching, but it forms the slot and hole for embedding a conductor at the part after forming an insulator layer previously, and consists of a conductor into it -- law is developed.
[0006] Next, the production process of drawing 10 explains the formation approach of wiring by the DAMASHIN method.
[0007] As shown in (1) of drawing 10 , the 2nd insulating layer 112 is formed on the 1st insulating layer 111. Even if formed by insulating material which is different in the 1st insulating layer 111 and 2nd insulating layer 112, it may be formed by the same insulating material.

[0008] Next, as shown in (2) of drawing 10 , the slot 113 for forming wiring or an electrode in the 2nd insulating layer 112 is formed with a usual lithography technique and a usual etching technique.
[0009] Then, as shown in (3) of drawing 10 , the barrier metal layer 114 is formed in the inside of this above-mentioned slot 113, and copper is further embedded as a conductor. then, the barrier metal layer 114 and copper which it began to see from the slot 113 -- chemical mechanical polishing (CMP [say / Following CMP] is the abbreviation for Chemical Mechanical Polishing) -- by law, it removes and flattening of the front face is carried out. Thus, the wiring 115 which consists of copper through the barrier metal layer 114 is formed in the interior of a slot 113. In this drawing, the barrier metal layer 114 is for preventing the diffusion (migration) to the 1st insulating layer 111 and 2nd insulating layer 112, and, as for current, a tantalum, an tantalum compound, or a tantalum alloy is used in many cases. Titanium, the titanium alloy, the tungsten, etc. are used with other ingredients.
[0010] Then, as shown in (4) of drawing 10 , a nitride (for example, silicon nitride film) 116 is formed on the 2nd insulating layer 112 so that the upper part of wiring 115 may be covered. This nitride 116 is for preventing the diffusion to the upper part of the copper under wiring 115.
[0011] the slot which embeds the upper wiring for a connection hole with lower layer wiring although above-mentioned drawing 10 showed the case where the wiring 115 which consists of copper was formed all over a slot 113, simultaneously dual DAMASHIN which forms and embeds a conductor at the slot and connection hole at coincidence -- it has the configuration with same barrier metal layer formed in Mizouchi and nitride formed on wiring also by law.
[0012] On the other hand, the trouble for using copper as an electrical conducting material is pointed out. That is, like aluminum, since copper is not various ingredients and the ingredient which forms an oxide easily, it moves easily in the inside of an interlayer insulation film and the insulator layer between wiring (diffusion). Therefore, in a semiconductor device, in order to realize copper wiring, the so-called formation of the barrier layer which prevents migration of copper becomes an indispensable technique. Therefore, it is necessary to prevent migration of copper certainly by the barrier layer.
[0013]
[Problem(s) to be Solved by the Invention] however, with the wiring structure explained by the Prior art Since there are few touch areas of the barrier metal layer formed in the inside of a wiring gutter and the nitride formed in the top face of copper wiring and the top face of copper wiring and the contact surface of a barrier metal layer and a nitride exist on the same flat surface mostly, For example, when a barrier metal layer and a nitride are removed by the stress of copper wiring, by it, the copper of copper wiring will move in the direction of the silicon oxide film from the interface of a barrier metal layer and a nitride. It is because it is the matter which copper tends [very] to move. It becomes the cause of leakage current, and that will cause a short circuit with adjoining copper wiring, when the worst.
[0014] Moreover, it is reported that the surface diffusion of copper of the interface and the various ingredients with which the laminating of two kinds of ingredients was carried out is very large. For example, in 1998 International Conference on SolidState Devices and Materials, S.U.Kim and others has reported the anomalous diffusion by which induction was carried out to the defect at the time of processing by the interface of BCB and a silicon nitride film. Thereby, in copper wiring, only thermal diffusion was understood that just minding is inadequate.
[0015]
[Means for Solving the Problem] This inventions are the semiconductor device made in order to solve the above-mentioned technical problem, and its manufacture approach.
[0016] In the semiconductor device which equipped with wiring the interior of the crevice which formed the semiconductor device in the interlayer insulation film, it has the 1st barrier layer which covers the wiring concerned from the lower part side of wiring, and the 2nd barrier layer which covers the wiring concerned from the upper part side of wiring, the 1st barrier layer and the 2nd barrier layers overlap, and wiring is covered.
[0017] The 1st barrier layer which covers the wiring concerned with the above-mentioned semiconductor device from the lower part side of wiring, Since it has the 2nd barrier layer which

covers the wiring concerned, the 1st barrier layer and the 2nd barrier layers overlap and wiring is covered from the upper part side of wiring, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer When the 1st barrier layer and the 2nd barrier layers overlap, even if one of barrier layers shift, the 1st barrier layer and the 2nd barrier layer hold contact in overlapping parts. That is, when the 1st barrier layer and the 2nd barrier layers overlap, a barrier layer comrade's adhesion force is strengthened. Therefore, the 1st barrier layer and the 2nd barrier layer separate, and the metal which constitutes wiring from the meantime does not move outside (or diffusion). Therefore, even if wiring is formed with copper or a copper alloy and the interlayer insulation film of silicon oxide is formed in the perimeter of wiring, the copper under wiring, for example, the ionized copper, does not move into an interlayer insulation film.

[0018] The process which forms wiring in the interior of a crevice by embedding a conductor while the manufacture approach of the 1st semiconductor device forms the 1st barrier layer in the inside of this crevice, after forming a crevice in an insulator layer, It is the manufacture approach equipped with the process which the insulator layer around wiring is removed [process] and makes wiring and the 1st barrier layer project from an insulator layer front face, and the process which overlaps the 1st barrier layer by the flank of wiring with a wrap in the upper part side of wiring, and forms the barrier layer of a wrap 2nd for wiring with the 1st barrier layer.

[0019] The process which forms wiring in the interior of a crevice by embedding a conductor while forming the 1st barrier layer in the inside of the crevice formed in the insulator layer by the manufacture approach of the 1st semiconductor device of the above, The process which the insulator layer around wiring is removed [process] and makes wiring and the 1st barrier layer project from an insulator layer front face, Since it has the process which overlaps the 1st barrier layer by the flank of wiring with a wrap in the upper part side of wiring, and forms the barrier layer of a wrap 2nd for wiring with the 1st barrier layer, wiring is covered with the 1st barrier layer and the 2nd barrier layer.

[0020] Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift when the 1st barrier layer and the 2nd barrier layers overlap, contact in the 1st barrier layer and the 2nd barrier layer will be maintained in overlapping parts. That is, a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer and the 2nd barrier layer may be overlapped. Therefore, since the 1st barrier layer and the 2nd barrier layer do not separate, the metal which a clearance opens in the meantime and constitutes wiring does not move outside (or diffusion). Therefore, even if it forms wiring with copper or a copper alloy, the copper under wiring does not move into an insulator layer.

[0021] The process which forms wiring in the interior of a crevice by embedding a conductor while the manufacture approach of the 2nd semiconductor device forms the 1st barrier layer in the inside of this crevice, after forming a crevice in an insulator layer, It is the manufacture approach equipped with the process which removes the insulator layer near the top section of the 1st barrier layer, and forms a slot, and the process which forms the 2nd barrier layer in the condition of embedding a slot for the upper part side of wiring with a wrap.

[0022] The process which forms wiring in the interior of a crevice by embedding a conductor while forming the 1st barrier layer in the inside of the crevice formed in the insulator layer by the manufacture approach of the 2nd semiconductor device of the above, Since it has the process which removes the insulator layer near the top section of the 1st barrier layer, and forms a slot, and the process which forms the 2nd barrier layer in the condition of embedding a slot for the upper part side of wiring with a wrap, wiring is covered with the 1st barrier layer and the 2nd barrier layer.

[0023] Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift when the 1st barrier layer and the 2nd barrier layers overlap, contact in the 1st barrier layer and the 2nd barrier layer will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer and the 2nd barrier layer may be overlapped. Therefore, since the 1st barrier layer and the 2nd barrier layer do not separate, the metal which a clearance opens in the meantime and constitutes wiring does not move outside (or diffusion). Therefore, even if it forms

wiring with copper or a copper alloy, the copper under wiring does not move into an insulator layer.
[0024] The process which forms wiring in the interior of a crevice by embedding a conductor while the manufacture approach of the 3rd semiconductor device forms the 1st barrier layer in the inside of this crevice, after forming a crevice in an insulator layer, It is the manufacture approach equipped with the process which removes the upper part of wiring so that it may become lower than an insulator layer front face, and the process which overlaps the 1st barrier layer in the top section of wiring with a wrap in the upper part side of wiring, and forms the barrier layer of a wrap 2nd for wiring with the 1st barrier layer.
[0025] The process which forms wiring in the interior of a crevice by embedding a conductor while forming the 1st barrier layer in the inside of the crevice formed in the insulator layer by the manufacture approach of the 3rd semiconductor device of the above, From having the process which removes the upper part of wiring so that it may become lower than an insulator layer front face, and the process which overlaps the 1st barrier layer in the top section of wiring with a wrap in the upper part side of wiring, and forms the barrier layer of a wrap 2nd for wiring with the 1st barrier layer Wiring is covered with the 1st barrier layer and the 2nd barrier layer.
[0026] Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift when the 1st barrier layer and the 2nd barrier layers overlap, contact in the 1st barrier layer and the 2nd barrier layer will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer and the 2nd barrier layer may be overlapped. Therefore, since the 1st barrier layer and the 2nd barrier layer do not separate, the metal which a clearance opens in the meantime and constitutes wiring does not move outside (or diffusion). Therefore, even if it forms wiring with copper or a copper alloy, the copper under wiring does not move into an insulator layer.
[0027]
[Embodiment of the Invention] The outline configuration sectional view of drawing 1 explains the gestalt of the 1st operation concerning the semiconductor device of this invention.
[0028] As shown in drawing 1 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. The above-mentioned interlayer insulation film 21 is formed with silicon oxide. It is formed in this wiring gutter 22 at the condition that wiring 24 projects from the top face of the above-mentioned interlayer insulation film 21 through the 1st barrier layer 23. Thus, the 1st barrier layer 23 has covered the above-mentioned wiring 24 from the lower part side. The 1st barrier layer 23 is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. The above-mentioned wiring 24 is formed with copper or a copper alloy.
[0029] The 2nd barrier layer 25 which furthermore covers the above-mentioned wiring 24 from an upper part side is formed in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0030] In addition, although it does not carry out illustration, the above-mentioned interlayer insulation film 21 may cover semiconductor devices, such as a transistor, capacity, and resistance, and wiring which were formed, for example on the semi-conductor substrate, may be a thing for flattening, or may cover a wiring layer. That is, it is the interlayer insulation film used for the usual semiconductor device.
[0031] The 1st barrier layer 23 which covers this wiring 24 with the gestalt of implementation of the above 1st from the lower part side of wiring 24, It has the 2nd barrier layer 25 which covers this wiring 24 from the upper part side of the above-mentioned wiring 24. Since the 1st barrier layer 23 and the 2nd barrier layers 25 overlap by the flank of wiring 24 and wiring 24 is covered, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 When the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, even if one of barrier layers (for example, 2nd barrier layer 25) shift, the 1st barrier layer 23 and the 2nd barrier layer 25 hold

contact in overlapping parts.
[0032] That is, when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, a barrier layer comrade's adhesion force is strengthened. Therefore, the 1st barrier layer 23 and the 2nd barrier layer 25 separate, and the metal which constitutes wiring 24 from the meantime does not move in the exterior of an interlayer insulation film 21, i.e., the direction, (or diffusion). That is, even if the stress of wiring 24 works, the condition of having covered wiring 24 with the 1st barrier layer 23 and the 2nd barrier layer 25 does not change. Therefore, the copper which constitutes wiring 24 ionizes, for example, and does not move into the interlayer insulation film 21 around wiring 24.

[0033] Next, the outline configuration sectional view of drawing 2 explains the gestalt of the 2nd operation concerning the semiconductor device of this invention. In addition, the same sign is given to the same component part as said drawing 1 in drawing 2 .
[0034] As shown in drawing 2 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. The above-mentioned interlayer insulation film 21 is formed with silicon oxide. Wiring 24 is formed in this wiring gutter 22 through the 1st barrier layer 23. Thus, the 1st barrier layer 23 has covered the above-mentioned wiring 24 from the lower part side. The 1st barrier layer 23 is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. The above-mentioned wiring 24 is formed with copper or a copper alloy.
[0035] The 2nd barrier layer 25 is formed so that a slot 26 may furthermore be formed in the interlayer insulation film 21 of the top section of the barrier layer 23 of the above 1st and the slot 26 may be embedded, and so that the above-mentioned wiring 24 may be covered from an upper part side. Thus, since the 2nd barrier layer 25 is formed, the 2nd barrier layer 25 is in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Or it is also possible to form by carbonization silicon, the tantalum, the tantalum alloy, tantalum nitride, etc. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0036] Since the 1st barrier layer 23 and the 2nd barrier layer 25 have covered wiring 24 with the gestalt of implementation of the above 2nd in the condition that the 1st barrier layer 23 and the 2nd barrier layers 25 overlap by the flank of wiring 24 It can prevent that the copper which constitutes wiring 24 ionizes the gestalt of said 1st operation, for example, and moves it into the interlayer insulation film 21 around wiring 24 similarly in the 1st barrier layer 23 and the 2nd barrier layer 25.
[0037] Next, the outline configuration sectional view of drawing 3 explains the gestalt of the 3rd operation concerning the semiconductor device of this invention. In addition, the same sign is given to the same component part as said drawing 1 in drawing 3 .
[0038] As shown in drawing 3 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. The above-mentioned interlayer insulation film 21 is formed with silicon oxide. Wiring 24 is formed in this wiring gutter 22 through the 1st barrier layer 23. Thus, the 1st barrier layer 23 has covered the above-mentioned wiring 24 from the lower part side. The 1st barrier layer 23 is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. The above-mentioned wiring 24 is formed with copper or a copper alloy.
[0039] The 2nd barrier layer 27 is formed so that a slot 26 may furthermore be formed in the interlayer insulation film 21 near the top section of the barrier layer 23 of the above 1st and the slot 26 may be embedded, and so that the above-mentioned wiring 24 may be covered from an upper part side. Thus, since the 2nd barrier layer 27 is formed, the 2nd barrier layer 27 is in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 27 is formed by low dielectric constant organic film like for example, the aryl ether as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 27.
[0040] In addition, the low dielectric constant organic film can be used for the barrier layer of the

above 2nd because the diffusion coefficient of the copper to the low dielectric constant organic film is small.

[0041] Since the 1st barrier layer 23 and the 2nd barrier layer 27 have covered wiring 24 with the gestalt of implementation of the above 3rd in the condition that the 1st barrier layer 23 and the 2nd barrier layers 27 overlap by the flank of wiring 24 It can prevent that the copper which constitutes wiring 24 ionizes the gestalt of said 1st operation, for example, and moves it into the interlayer insulation film 21 around wiring 24 similarly in the 1st barrier layer 23 and the 2nd barrier layer 27. Moreover, the 2nd barrier layer 27 can be used as an interlayer insulation film during wiring with wiring 24 and wiring (not shown) formed in the upper part.

[0042] Next, the outline configuration sectional view of drawing 4 explains the gestalt of the 4th operation concerning the semiconductor device of this invention. In addition, the same sign is given to the same component part as said drawing 1 in drawing 4 .

[0043] As shown in drawing 4 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. The above-mentioned interlayer insulation film 21 is formed with silicon oxide. The 1st barrier layer 23 is formed in the wall (a pars basilaris ossis occipitalis is also included) of this wiring gutter 22. The barrier layer 23 of the above 1st is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. Furthermore, it is formed in the above-mentioned wiring gutter 22 at the condition of having dented wiring 24 from the top face of the above-mentioned interlayer insulation film 21 through the barrier layer 23 of the above 1st. This wiring 24 is formed with copper or a copper alloy.

[0044] Therefore, the barrier layer 23 of the above 1st is formed also on the side of the above-mentioned wiring 24 in the above-mentioned wiring gutter 22, and the lower part side of the above-mentioned wiring 24 is covered with the 1st barrier layer 23.

[0045] The 2nd barrier layer 25 which furthermore covers the above-mentioned wiring 24 from an upper part side is formed in the condition of overlapping by the barrier layer 23 of the above 1st, and the side attachment wall of the above-mentioned wiring gutter 22. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.

[0046] In addition, although it does not carry out illustration, the above-mentioned interlayer insulation film 21 may cover semiconductor devices, such as a transistor, capacity, and resistance, and wiring which were formed, for example on the semi-conductor substrate, may be a thing for flattening, or may cover a wiring layer. That is, it is the interlayer insulation film used for the usual semiconductor device.

[0047] The 1st barrier layer 23 which covers this wiring 24 with the gestalt of implementation of the above 4th from the lower part side of wiring 24, It has the 2nd barrier layer 25 which covers this wiring 24 from the upper part side of the above-mentioned wiring 24. Since the 1st barrier layer 23 and the 2nd barrier layers 25 overlap by the flank of a wiring gutter 22 and wiring 24 is covered, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 When the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, even if one of barrier layers (for example, 2nd barrier layer 25) shift, contact in the 1st barrier layer 23 and the 2nd barrier layer 25 will be held in overlapping parts.

[0048] That is, when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, a barrier layer comrade's adhesion force is strengthened. Therefore, the 1st barrier layer 23 and the 2nd barrier layer 25 separate, and the metal which constitutes wiring 24 from the meantime does not move in the exterior of an interlayer insulation film 21, i.e., the direction, (or diffusion). That is, even if the stress of wiring 24 works, the condition of having covered wiring 24 with the 1st barrier layer 23 and the 2nd barrier layer 25 does not change. Therefore, the copper which constitutes wiring 24 ionizes, for example, and does not move into the interlayer insulation film 21 around wiring 24.

[0049] Next, the production process Fig. of drawing 5 explains the gestalt of the operation concerning the 1st manufacture approach of this invention. The same sign is given to the component part which showed as an example the manufacture approach of the semiconductor

device explained by said drawing 1 , and was shown by said drawing 1 , and the same components in drawing 5 .

[0050] As shown in (1) of drawing 5 , semiconductor devices (for example, a transistor, capacity, resistance, etc.) are formed in a semi-conductor substrate (illustration abbreviation), and lower layer wiring, a circuit pattern, etc. are further formed in it. On such a semi-conductor substrate, the wrap insulator layer 11 is formed in those components, wiring, etc. An interlayer insulation film 21 is formed on the insulator layer 11. This interlayer insulation film 21 is formed by the cascade screen of low dielectric constant organic film, such as for example, the aryl ether, and the silicon oxide film. Or it forms by the so-called low dielectric constant film, such as a cascade screen of the fluororesin film and the silicon oxide film, fluorine oxide-ized silicon film, organic SOG film, and inorganic SOG film. It is required for a design rule to contain the low dielectric constant film with the device after 0.13-micrometer generation especially.

[0051] then, DAMASHIN generally known -- after forming a crevice (it explains as a wiring gutter hereafter) 22 in an interlayer insulation film 21, the 1st barrier layer 23 is formed in the inside of a wiring gutter 22 by tantalum nitride or the tantalum by law as an ingredient which has barrier property to a copper atom and a copper ion. Furthermore, after forming a copper seed layer in the inside of a wiring gutter 22 through the 1st barrier layer 23, the interior of a wiring gutter 22 is embedded with a conductor (for example, copper) by the electrolysis galvanizing method etc. Then, for example by CMP, the excessive copper on an interlayer insulation film 21 and the 1st barrier layer 23 are removed, and the wiring 24 which becomes the interior of a wiring gutter 22 from copper through the 1st barrier layer 23 is formed.

[0052] Next, etching removes the interlayer insulation film 21 around wiring 24, and wiring 24 and the 1st barrier layer 23 are made to project from the front face of an interlayer insulation film 21, as shown in (2) of drawing 5 . Therefore, the 1st barrier layer 23 is in the condition of having covered the above-mentioned wiring 24 from the lower part side.

[0053] By the above-mentioned etching, when an interlayer insulation film 21 is silicon oxide film, wet etching removes here [the fluoric acid water solution and here] whose concentration is 0.1% - 1.0%, using 0.5% of fluoric acid water solution as an example. In addition, since an etching rate becomes late in the wet etching using the fluoric acid water solution of less than 0.1% of concentration, it is not practical, and since a metal part will also be etched in the wet etching using the fluoric acid water solution exceeding 1.0%, it is not desirable. Moreover, in the case of low dielectric constant organic film like the aryl ether, an interlayer insulation film 21 removes by hydrogen plasma etching or nitrogen plasma etching. In addition, since the copper of wiring 24 is oxidized and it becomes a defect's cause, it is not desirable to use oxygen plasma etching. Moreover, it is desirable to perform from a viewpoint of antioxidizing of wiring 24 to formation of the 2nd barrier layer performed to this etching and degree by the non-oxidizing atmosphere. Namely, the so-called in situ Processing is desirable.

[0054] Moreover, it is also possible to perform etching of the above-mentioned interlayer insulation film 21 by the dry etching using the gas of a carbon fluoride system. In this case, the upper part of the 1st barrier layer 23 may also be etched. In addition, even if the upper part of the 1st barrier layer 23 is etched, it is necessary to perform the above-mentioned etching so that the amount of laps to the 1st barrier layer 23 of the 2nd barrier layer formed after that can fully secure, namely, so that it may leave the 1st barrier layer 23 to height of 30nm or more from the front face of the interlayer insulation film 21 after etching.

[0055] It is desirable to form the height of the level difference of an interlayer insulation film 21 and the 1st barrier layer 23 in at least 30nm or more by etching of the above-mentioned interlayer insulation film 21. It is because a lap part with the 2nd barrier layer formed behind decreases, it becomes difficult to secure sufficient barrier property and it becomes being the same as that of the structure of the conventional barrier layer, when the above-mentioned level difference is 30nm or less.

[0056] Next, as shown in (3) of drawing 5 , the 2nd barrier layer 25 is formed on the above-mentioned interlayer insulation film 21 so that the above-mentioned wiring 24 may be covered. This 2nd barrier layer 25 is formed by insulator layers, such as silicon nitride and hydrogenation silicon carbon, as an ingredient which has barrier property to a copper atom and a copper ion. As

the manufacture approach, a CVD method is desirable. As the other membrane formation approaches, the membrane formation approaches, such as sputtering and a sol gel process, can also be used. When forming membranes with a CVD method, it is etching and in situ of the above-mentioned interlayer insulation film 21. Processing is desirable. for example, etching using the hydrogen plasma after etching the silicon oxide film in a rare fluoric acid water solution -- about [5nm-20nm] etching -- carrying out -- after that -- continuing -- chemical vapor growth (CVD [say / the following and CVD] is the abbreviation for Chemical Vapour Deposition) -- the 2nd barrier layer 25 which consists of a silicon nitride film by law is formed.

[0057] When an interlayer insulation film 21 is organic film, 10nm - about 100nm is etched by etching which used the hydrogen plasma or the nitrogen plasma, and the 2nd barrier layer 25 is formed with a silicon nitride film with a CVD method after that. As for a silicon nitride film, at this time, it is desirable to form in the thickness of 20nm - about 100nm. Barrier property sufficient in less than 20nm is not obtained. On the other hand by the thickness exceeding 100nm, the capacity between wiring becomes large, and it is not desirable. Thus, by etching using the hydrogen plasma, the oxide film (copper oxide film) of the front face of wiring 24 is etched, the front face of wiring 24 is cleaned to coincidence, and adhesion with the 2nd barrier layer 25 which consists of a silicon nitride film improves.

[0058] Moreover, in case the 2nd barrier layer 25 which consists of a silicon nitride film with a CVD method is formed, it is desirable to form so that the thickness of the side attachment wall of wiring 24 may become thin rather than the thickness on wiring 24. If a silicon nitride film is formed between wiring, since the capacity between wiring will rise, it is for controlling the rise of the capacity between wiring as much as possible. Therefore, it is good to form membranes in a CVD method, using high density plasma-CVD equipment as a CVD method which has directivity. Or it is good to form membranes using parallel monotonous mold plasma-CVD equipment. As the membrane formation condition, a step hippo ridge considers as the conditions used as about 30% or less. As membrane formation conditions at the time of using parallel monotonous mold plasma-CVD equipment, as an example, 1.03kPa(s) and membrane formation temperature are set as 400 degrees C, and a process gas ratio is set as about mono-silane [SiH4]:ammonia (NH3) =3:1 for the pressure of a membrane formation ambient atmosphere. Furthermore, it is desirable to perform plasma treatment which includes either [at least] the hydrogen plasma or the nitrogen plasma just before CVD. As membrane formation conditions at the time of using high density plasma-CVD equipment, as an example, 1Pa or less and membrane formation temperature are set as 200 degrees C - 400 degrees C, and a process gas ratio is set as about mono-silane [SiH4]:nitrogen (N2) =3:1.5-5 for the pressure of a membrane formation ambient atmosphere.

[0059] If the 2nd barrier layer 25 is formed as mentioned above, the 2nd barrier layer 25 will overlap the 1st barrier layer 23 by the flank of wiring 24 with a wrap in the upper part side of wiring 24, and will cover wiring 24 with the 1st barrier layer 23.

[0060] Then, as shown in (4) of drawing 5 , an interlayer insulation film 31 is formed on the 2nd barrier layer 25. As for an interlayer insulation film 31, it is desirable to include the low dielectric constant film. Although the aryl ether was used in this invention, otherwise, it is possible to use organic [SOG], inorganic [SOG], a fluororesin, xerogel, etc.

[0061] In addition, although illustration is not carried out, the plug is formed in the location to a connection hole and its interior predetermined [of the above-mentioned insulator layer 11]. Moreover, in forming wiring 24 by the dual DAMASHIN method, in case a connection hole is formed in the position of the above-mentioned insulator layer 11 by the dual DAMASHIN method and it forms wiring 24, the conductor which forms wiring 24, for example, copper, is embedded, and a plug is formed also in the interior of a connection hole.

[0062] By the 1st manufacture approach explained by above-mentioned drawing 5 After forming in the interior of a wiring gutter 22 the wiring 24 which consists of copper through the 1st barrier layer 23, the interlayer insulation film 21 around wiring 24 is removed. Wiring 24 and the 1st barrier layer 23 are made to project from the front face of an interlayer insulation film 21. Then, since the 1st barrier layer 23 is overlapped by the flank of wiring 24 with a wrap in the upper part side of wiring 24 and the barrier layer 25 of a wrap 2nd is formed for wiring 24 with the 1st

barrier layer 23, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0063] Therefore, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 and one of barrier layers shift when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, contact in the 1st barrier layer 23 and the 2nd barrier layer 25 will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer 23 and the 2nd barrier layer 25 may be overlapped. Therefore, since the 1st barrier layer 23 and the 2nd barrier layer 25 do not separate, the copper which a clearance opens in the meantime and constitutes wiring 24 does not move outside (or diffusion). Therefore, even if it forms wiring 24 with copper (or copper alloy) as mentioned above and uses the silicon oxide film for the above-mentioned interlayer insulation film 21, the copper under wiring 24, for example, the ionized copper, does not move into an interlayer insulation film 21.
[0064] Moreover, in the manufacture approach of the above 1st, the interlayer insulation film 21 has a laminated structure of the low dielectric constant organic film and the silicon oxide film. The upper part of an interlayer insulation film 21 is formed by the silicon oxide film, and when the thickness of the silicon oxide film is 30nm - about 100nm In order to make wiring 24 and the 1st barrier layer 23 project, in the process which removes the upper part of an interlayer insulation film 21, all the silicon oxide film parts of an interlayer insulation film 21 may be removed.
[0065] Next, the production process Fig. of drawing 6 explains the gestalt of the 1st operation concerning the 2nd manufacture approach of this invention. The same sign is given to the component part which showed as an example the manufacture approach of the semiconductor device explained by said drawing 2 , and was shown by said drawing 2 , and the same components in drawing 6 .
[0066] the approach same as shown in (1) of drawing 6 , i.e., DAMASHIN generally known, as (1) of said drawing 5 explained -- after forming a crevice (it explains as a wiring gutter hereafter) 22 in an interlayer insulation film 21, the 1st barrier layer 23 is formed in the inside of a wiring gutter 22 by tantalum nitride or the tantalum by law as an ingredient which has barrier property to a copper atom and a copper ion. Furthermore, after forming a copper seed layer in the inside of a wiring gutter 22 through the 1st barrier layer 23, the interior of a wiring gutter 22 is embedded with a conductor (for example, copper) by the electrolysis galvanizing method etc. Then, for example by CMP, the excessive copper on an interlayer insulation film 21 and the 1st barrier layer 23 are removed, and the wiring 24 which becomes the interior of a wiring gutter 22 from copper through the 1st barrier layer 23 is formed.
[0067] Subsequently, as shown in (2) of drawing 6 , an interlayer insulation film 21 is etched. Conditions into which the interlayer insulation film 21 in the side periphery of the 1st barrier layer 23 is etched in the etching conditions in that case are chosen. In for example, the case of the silicon oxide film with which an interlayer insulation film 21 contains 10% - 20% of carbon a magnetron mold etching system -- using -- etching gas -- an argon [trifluoromethane / (CHF3) / [a supply flow rate is set for example, to 5sccm(s)]] -- an oxygen (O2) [supply flow rate is set [(Ar / [a supply flow rate is set) for example, to 20sccm(s)]] for example, to 5sccm (s) --] -- using -- What is necessary is to set the pressure of an etching ambient atmosphere as 5Pa, to set impression power as 600W, and just to carry out whole surface etchback of the interlayer insulation film 21 as an example. A slot 26 is formed in the interlayer insulation film 21 near the top section of the barrier layer 23 of the above 1st by carrying out etchback on such conditions.
[0068] Then, as shown in (3) of drawing 6 , the 2nd barrier layer 25 is formed so that the above-mentioned slot 26 may be embedded, and so that the above-mentioned wiring 24 may be covered from an upper part side. Thus, since the 2nd barrier layer 25 is formed, the 2nd barrier layer 25 will be in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0069] With the gestalt of the 1st operation concerning the 2nd manufacture approach explained by above-mentioned drawing 6 Wiring 24 is formed in the interior of the wiring gutter 22 formed

in the interlayer insulation film 21 through the 1st barrier layer 23. Subsequently, since the 2nd barrier layer 25 is formed in the condition of embedding a slot 26 for the upper part side of wiring 24 with a wrap after removing the interlayer insulation film 21 near the top section of the 1st barrier layer 23 and forming a slot 26, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.

[0070] Therefore, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 and one of barrier layers shift when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, contact in the 1st barrier layer 23 and the 2nd barrier layer 25 will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer 23 and the 2nd barrier layer 25 may be overlapped. Therefore, since the 1st barrier layer 23 and the 2nd barrier layer 25 do not separate, the copper which a clearance opens in the meantime and constitutes wiring 24 does not move outside (or diffusion). Therefore, even if it forms wiring 24 with copper (or copper alloy) as mentioned above and uses the silicon oxide film for the above-mentioned interlayer insulation film 21, the copper under wiring 24, for example, the ionized copper, does not move into an interlayer insulation film 21.

[0071] Next, the production process Fig. of drawing 7 explains the gestalt of the 2nd operation concerning the 2nd manufacture approach of this invention. The same sign is given to the component part which showed as an example the manufacture approach of the semiconductor device explained by said drawing 3 , and was shown by said drawing 3 , and the same components in drawing 7 .

[0072] By the same approach, a crevice (it explains as a wiring gutter hereafter) 22 is formed in an interlayer insulation film 21, and the wiring 24 which becomes the interior of the wiring gutter 22 from copper through the 1st barrier layer 23 is formed as (1) of said drawing 6 and (2) explained. Subsequently, etchback of the interlayer insulation film 21 is carried out, and a slot 26 is formed in the interlayer insulation film 21 of the top section of the barrier layer 23 of the above 1st.

[0073] Then, as are shown in drawing 7 , and the above-mentioned wiring 24 is covered from an upper part side so that the above-mentioned slot 26 may be embedded and, the 2nd barrier layer 27 is formed on an interlayer insulation film 21. This 2nd barrier layer 27 is formed by low dielectric constant organic film like for example, the aryl ether as an ingredient which has barrier property to a copper atom and a copper ion. Thus, the 2nd barrier layer 27 is formed in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24.

[0074] Therefore, the same operation effectiveness as the gestalt of implementation of the above 1st is acquired. That is, since wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 17 even if it forms wiring 24 with copper (or copper alloy) as mentioned above and therefore uses the silicon oxide film for the above-mentioned interlayer insulation film 21, the copper under wiring 24, for example, the ionized copper, does not move into an interlayer insulation film 21.

[0075] Next, the production process Fig. of drawing 8 explains the gestalt of the operation concerning the 3rd manufacture approach of this invention. The same sign is given to the component part which showed as an example the manufacture approach of the semiconductor device explained by said drawing 4 , and was shown by said drawing 4 , and the same components in drawing 8 .

[0076] As shown in (1) of drawing 8 , semiconductor devices (for example, a transistor, capacity, resistance, etc.) are formed in a semi-conductor substrate (illustration abbreviation), and lower layer wiring, a circuit pattern, etc. are further formed in it. On such a semi-conductor substrate, the wrap insulator layer 11 is formed in those components, wiring, etc. An interlayer insulation film 21 is formed on the insulator layer 11. This interlayer insulation film 21 is formed by the cascade screen of organic film, such as for example, the aryl ether, and the silicon oxide film. Or it forms by the so-called low dielectric constant film, such as a cascade screen of the fluororesin film and the silicon oxide film, fluorine oxide-ized silicon film, organic SOG film, and inorganic SOG film. It is required for a design rule to contain the low dielectric constant film with

the device after 0.13-micrometer generation especially.
[0077] then, DAMASHIN generally known -- after forming a crevice (it explains as a slot below) in an interlayer insulation film 21, the 1st barrier layer 23 is formed in the inside of a wiring gutter 22 by tantalum nitride or the tantalum by law as an ingredient which has barrier property to a copper atom and a copper ion. Furthermore, after forming a copper seed layer in the inside of a wiring gutter 22 through the 1st barrier layer 23, the interior of a wiring gutter 22 is embedded with a conductor (for example, copper) by the electrolysis galvanizing method etc. Then, for example by CMP, the excessive copper on an interlayer insulation film 21 and the 1st barrier layer 23 are removed, and the wiring 24 which becomes the interior of a wiring gutter 22 from copper through the 1st barrier layer 23 is formed.
[0078] Next, as shown in (2) of drawing 8 , only the upper part where the top face of wiring 24 becomes low rather than the front face of an interlayer insulation film 21 and which is wiring 24 that it will be is etched alternatively. It is desirable to form the height of the level difference of wiring 24 and the 1st barrier layer 23 in at least 30nm or more by the above-mentioned etching. It is because a lap part with the 2nd barrier layer formed behind decreases, it becomes difficult to secure sufficient barrier property and it becomes being the same as that of the structure of the conventional barrier layer, when the above-mentioned level difference is 30nm or less.
[0079] Subsequently, as shown in (3) of drawing 8 , sputter etching or hydrogen plasma etching removes the front face of wiring 24 for an oxide film etc. Then, for example by sputtering, the 2nd barrier layer 25 is formed on an interlayer insulation film 21 so that wiring 24 may be covered. The barrier layer 25 of the above 2nd is formed by the tantalum, tantalum nitride, etc. as an ingredient which has barrier property to a copper atom and a copper ion. As the other membrane formation approaches, it is also possible to use the membrane formation approaches, such as a steamy method and a CVD method.
[0080] In addition, in order not to make the front face of wiring 24 generate an oxide film, it is desirable to perform the period until it forms the 2nd barrier layer 25 from the above-mentioned sputter etching or hydrogen plasma etching by the non-oxidizing atmosphere. For example, the so-called in situ Processing is desirable. For example, by sputter etching, 5nm - about 20nm is etched, and the 2nd barrier layer 25 which consists of tantalum film by sputtering continuously is formed after that. As for this tantalum film, it is desirable to form in the thickness of 20nm - about 75nm. Barrier property sufficient in less than 20nm is not obtained. On the other hand, by the thickness exceeding 75nm, processing will take time amount and wiring resistance will become large too much.
[0081] Then, as shown in (4) of drawing 8 , CMP removes the 2nd barrier layer 25 on an interlayer insulation film 21. Consequently, the configuration whose 1st barrier layer 23 and 2nd barrier layer 25 overlap in the top section of wiring 24, and cover wiring 24 with the 1st barrier layer 23 and the 2nd barrier layer 25 in a wiring gutter 22 is completed. Thus, since the 2nd barrier layer 25 on an interlayer insulation film 21 is removed, it becomes possible to form the 2nd barrier layer 25 by the tantalum nitride and the tantalum of a conductor.
[0082] Then, although illustration is not carried out, an interlayer insulation film 31 is formed on the 2nd barrier layer 25 and an interlayer insulation film 21 like said 1st manufacture approach. As for an interlayer insulation film 31, it is desirable to include the low dielectric constant film. Although the aryl ether was used in this invention, otherwise, it is possible to use organic [SOG], inorganic [SOG], a fluororesin, xerogel, etc.
[0083] In addition, it is also possible to form the barrier layer 25 of the above 2nd by insulator layers, such as a silicon nitride film explained by said 1st manufacture approach and hydrogenation silicon carbon. The membrane formation approach in that case, membrane formation conditions, etc. are the same with having explained by the 1st manufacture approach.
[0084] Moreover, in the manufacture approach of the above 3rd, although illustration is not carried out, the plug is formed in the location to a connection hole and its interior predetermined [of the above-mentioned insulator layer 11]. Moreover, in forming wiring 24 by the dual DAMASHIN method, in case a connection hole is formed in the position of the above-mentioned insulator layer 11 by the dual DAMASHIN method and it forms wiring 24, the conductor which forms wiring 24, for example, copper, is embedded, and a plug is formed also in the interior of a

connection hole.
[0085] By the 2nd manufacture approach explained by above-mentioned drawing 8 After forming in the interior of a wiring gutter 22 the wiring 24 which consists of copper through the 1st barrier layer 23, the upper part of wiring 24 is removed. Make the top face of wiring 24 lower than the front face of an interlayer insulation film 21, overlap the 1st barrier layer 23 by the flank of wiring 24 with a wrap in the upper part side of wiring 24 after that, and wiring 24 from forming the barrier layer 25 of a wrap 2nd with the 1st barrier layer 23 Wiring 24 comes to be covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0086] Therefore, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 and one of barrier layers shift when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, contact in the 1st barrier layer 23 and the 2nd barrier layer 25 will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer 23 and the 2nd barrier layer 25 may be overlapped. Therefore, since the 1st barrier layer 23 and the 2nd barrier layer 25 do not separate, the copper which a clearance opens in the meantime and constitutes wiring 24 does not move outside (or diffusion). Therefore, even if it forms wiring 24 with copper (or copper alloy) as mentioned above and uses the silicon oxide film for the above-mentioned interlayer insulation film 21, the copper under wiring 24, for example, the ionized copper, does not move into an interlayer insulation film 21.
[0087] In addition, it is also possible to consider as the structure concerning the semiconductor device of this invention as shown in drawing 9 as a gestalt of the 5th operation. It is explained below.
[0088] As shown in drawing 9 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. It is formed in this wiring gutter 22 at the condition that wiring 24 projects from the top face of the above-mentioned interlayer insulation film 21 through the 1st barrier layer 23. And the 1st barrier layer 23 is formed also on the interlayer insulation film 21 around a wiring gutter 22. Thus, in order to form, after removing the conductor (for example, copper) for forming wiring deposited on the 1st barrier layer 23 in CMP, it is necessary to carry out patterning of the 1st barrier layer 23 according to the so-called mask process (a lithography technique and etching). In addition, the barrier layer 23 of the above 1st is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. The above-mentioned wiring 24 is formed with copper or a copper alloy.
[0089] The 2nd barrier layer 25 which furthermore covers the above-mentioned wiring 24 from an upper part side is formed in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0090] Also with the gestalt of implementation of the above 5th, the same effectiveness as said 1st explained operation gestalt is acquired.
[0091] When the lap width of face in the lengthwise direction of a wiring cross section with the 1st barrier layer 23, the 2nd barrier layer 25, or the 2nd barrier layer 27 explained with the gestalt of each above-mentioned implementation was required however had the thickness in the side face of the wiring 24 of the 1st barrier layer 23, or the side face of a wiring gutter 22, and more than comparable [about 45nm / a maximum of], it came out enough and a certain thing was checked by experiment of an artificer.
[0092] The 1st barrier layer 23 and the 2nd barrier layer 25, or the 2nd barrier layer 27 explained with the gestalt of each above-mentioned implementation can be applied also to a dual pellet syn conformation.
[0093] Moreover, even if it is the configuration which made vertical reverse the configuration explained with the gestalt of each above-mentioned implementation, it enters under the category of this invention.
[0094]
[Effect of the Invention] As mentioned above, since according to the semiconductor device of

this invention the lower part of wiring is covered with the 1st barrier layer, the upper part side of wiring is covered with the 2nd barrier layer, as explained, and the 1st barrier layer and the 2nd barrier layers overlap Even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift, the 1st barrier layer and the 2nd barrier layer cannot estrange, and wiring can always be covered with the 1st barrier layer and the 2nd barrier layer. Therefore, even if wiring is formed with copper or a copper alloy, the copper under wiring cannot move out of wiring. Therefore, short generating during wiring and generating of leakage current can be suppressed, and it becomes what has high wiring dependability.

[0095] According to the manufacture approach of the 1st semiconductor device concerning this invention, the insulator layer around wiring formed in the crevice formed in the insulator layer by embedding a conductor is removed. After making wiring and the 1st barrier layer project from an insulator layer front face, since the barrier layer of a wrap 2nd is formed with the 1st barrier layer, wiring by overlapping the 1st barrier layer by the flank of wiring with a wrap in the upper part side of wiring Wiring can be completely covered with the 1st barrier layer and the 2nd barrier layer. Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift, even if it forms wiring with copper or a copper alloy since contact in the 1st barrier layer and the 2nd barrier layer can be maintained in overlapping parts, migration of the copper under wiring can be prevented. Therefore, the thing which has high wiring dependability and which suppressed short generating during wiring and generating of leakage current can be manufactured.

[0096] After according to the manufacture approach of the 2nd semiconductor device concerning this invention removing the insulator layer near the top section of the 1st barrier layer in the crevice formed in the insulator layer and forming a slot, Since cover the upper part side of wiring, and a slot is embedded, the 1st barrier layer is overlapped by the flank of wiring and the barrier layer of a wrap 2nd is formed for wiring with the 1st barrier layer, wiring can be completely covered with the 1st barrier layer and the 2nd barrier layer. Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift, even if it forms wiring with copper or a copper alloy since contact in the 1st barrier layer and the 2nd barrier layer can be maintained in overlapping parts, migration of the copper under wiring can be prevented. Therefore, the thing which has high wiring dependability and which suppressed short generating during wiring and generating of leakage current can be manufactured.

[0097] The upper part of wiring formed by embedding the crevice conductor formed in the insulator layer according to the manufacture approach of the 3rd semiconductor device concerning this invention is removed. Since the 1st barrier layer is overlapped in the top section of wiring with a wrap in the upper part side of wiring and the barrier layer of a wrap 2nd is formed for wiring with the 1st barrier layer after forming lower than an insulator layer front face, wiring can be completely covered with the 1st barrier layer and the 2nd barrier layer. Therefore, as well as the manufacture approach of the above 1st even if it forms wiring with copper or a copper alloy, migration of the copper under wiring, for example, the ionized copper, can be prevented. Therefore, the thing which has high wiring dependability and which suppressed short generating during wiring and generating of leakage current can be manufactured.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] This invention relates to the semiconductor device which used copper or a copper alloy for the conductor, and its manufacture approach in detail about a semiconductor device and its manufacture approach.

[Translation done.]

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PRIOR ART

[Description of the Prior Art] Contraction-ization of detailed-izing of wiring and a wiring pitch is needed with detailed-izing of a semiconductor device. Moreover, the reduction in the dielectric constant of an interlayer insulation film and low resistance-ization of wiring have been needed for coincidence with the demand of low-power-izing, improvement in the speed, etc. In the logic device, since a resistance rise especially according to detailed wiring and the increment in wiring capacity lead to the fall of the working speed of a device, the multilayer interconnection using an interlayer insulation film made detailed is needed in the low dielectric constant film.
[0003] It has caused increase of the number of processes at the same time contraction-ization of detailed-izing of wiring width of face and a pitch enlarges the aspect ratio of spacing during wiring (Rhine - and tooth-space part of - tooth space), and a burden is placed on the technique which forms long and slender detailed wiring perpendicularly as a result, the technique which embeds between detailed wiring with an interlayer insulation film and it not only enlarges the aspect ratio of the wiring [itself], but it complicates a process.
[0004] It is possible for it not to be necessary to embed a connection hole (for example, beer hall) and a wiring gutter by reflow sputtering of metals (aluminum, copper, etc.) or plating at coincidence, and for forming metal wiring of a high aspect ratio by etching not to embed **** during wiring with an interlayer insulation film in the DAMASHIN process which grinds a surface metal by chemical mechanical polishing (it is called Following CMP), either, and to reduce the number of processes sharply. This process comes to contribute to reduction of the total manufacturing cost greatly, so that the aspect ratio of wiring becomes high and a wiring total increases.
[0005] Conventionally, in wiring of LSI, although aluminum and an aluminium alloy have been used for the electrical conducting material, in order to attain improvement in the speed and low-power-ization with improvement in the degree of integration of a semiconductor integrated circuit in recent years, a copper alloy has come to be used for an electrical conducting material. moreover, DAMASHIN embedding the wiring material which the manufacture approach of using copper for a wiring material does not make an insulator layer cover after processing a wiring material by the conventional etching, but it forms the slot and hole for embedding a conductor at the part after forming an insulator layer previously, and consists of a conductor into it -- law is developed.
[0006] Next, the production process of drawing 10 explains the formation approach of wiring by the DAMASHIN method.
[0007] As shown in (1) of drawing 10 , the 2nd insulating layer 112 is formed on the 1st insulating layer 111. Even if formed by insulating material which is different in the 1st insulating layer 111 and 2nd insulating layer 112, it may be formed by the same insulating material.
[0008] Next, as shown in (2) of drawing 10 , the slot 113 for forming wiring or an electrode in the 2nd insulating layer 112 is formed with a usual lithography technique and a usual etching technique.
[0009] Then, as shown in (3) of drawing 10 , the barrier metal layer 114 is formed in the inside of this above-mentioned slot 113, and copper is further embedded as a conductor. then, the barrier metal layer 114 and copper which it began to see from the slot 113 -- chemical mechanical

polishing (CMP [say / Following CMP] is the abbreviation for Chemical Mechanical Polishing) -- by law, it removes and flattening of the front face is carried out. Thus, the wiring 115 which consists of copper through the barrier metal layer 114 is formed in the interior of a slot 113. In this drawing, the barrier metal layer 114 is for preventing the diffusion (migration) to the 1st insulating layer 111 and 2nd insulating layer 112, and, as for current, a tantalum, an tantalum compound, or a tantalum alloy is used in many cases. Titanium, the titanium alloy, the tungsten, etc. are used with other ingredients.

[0010] Then, as shown in (4) of drawing 10 , a nitride (for example, silicon nitride film) 116 is formed on the 2nd insulating layer 112 so that the upper part of wiring 115 may be covered. This nitride 116 is for preventing the diffusion to the upper part of the copper under wiring 115.

[0011] the slot which embeds the upper wiring for a connection hole with lower layer wiring although above-mentioned drawing 10 showed the case where the wiring 115 which consists of copper was formed all over a slot 113, simultaneously dual DAMASHIN which forms and embeds a conductor at the slot and connection hole at coincidence -- it has the configuration with same barrier metal layer formed in Mizouchi and nitride formed on wiring also by law.

[0012] On the other hand, the trouble for using copper as an electrical conducting material is pointed out. That is, like aluminum, since copper is not various ingredients and the ingredient which forms an oxide easily, it moves easily in the inside of an interlayer insulation film and the insulator layer between wiring (diffusion). Therefore, in a semiconductor device, in order to realize copper wiring, the so-called formation of the barrier layer which prevents migration of copper becomes an indispensable technique. Therefore, it is necessary to prevent migration of copper certainly by the barrier layer.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, it is since according to the semiconductor device of this invention the lower part of wiring is covered with the 1st barrier layer, the upper part side of wiring is covered with the 2nd barrier layer and the 1st barrier layer and the 2nd barrier layers overlap, as explained, Even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift, the 1st barrier layer and the 2nd barrier layer cannot estrange, and wiring can always be covered with the 1st barrier layer and the 2nd barrier layer. Therefore, even if wiring is formed with copper or a copper alloy, the copper under wiring cannot move out of wiring. Therefore, short generating during wiring and generating of leakage current can be suppressed, and it becomes what has high wiring dependability.
[0095] According to the manufacture approach of the 1st semiconductor device concerning this invention, the insulator layer around wiring formed in the crevice formed in the insulator layer by embedding a conductor is removed, Since the 1st barrier layer is overlapped by the flank of wiring with a wrap in the upper part side of wiring and the barrier layer of a wrap 2nd is formed for wiring with the 1st barrier layer after making wiring and the 1st barrier layer project from an insulator layer front face, wiring can be completely covered with the 1st barrier layer and the 2nd barrier layer. Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift, even if it forms wiring with copper or a copper alloy since contact in the 1st barrier layer and the 2nd barrier layer can be maintained in overlapping parts, migration of the copper under wiring can be prevented. Therefore, the thing which has high wiring dependability and which suppressed short generating during wiring and generating of leakage current can be manufactured.
[0096] According to the manufacture approach of the 2nd semiconductor device concerning this invention, the insulator layer near the top section of the 1st barrier layer in the crevice formed in the insulator layer is removed. Since cover the upper part side of wiring, and a slot is embedded, the 1st barrier layer is overlapped by the flank of wiring and the barrier layer of a wrap 2nd is formed for wiring with the 1st barrier layer after forming a slot, wiring can be completely covered with the 1st barrier layer and the 2nd barrier layer. Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift, even if it forms wiring with copper or a copper alloy since contact in the 1st barrier layer and the 2nd barrier layer can be maintained in overlapping parts, migration of the copper under wiring can be prevented. Therefore, the thing which has high wiring dependability and which suppressed short generating during wiring and generating of leakage current can be manufactured.
[0097] According to the manufacture approach of the 3rd semiconductor device concerning this invention, the upper part of wiring formed by embedding the crevice conductor formed in the insulator layer is removed, Since the 1st barrier layer is overlapped in the top section of wiring with a wrap in the upper part side of wiring and the barrier layer of a wrap 2nd is formed for wiring with the 1st barrier layer after forming lower than an insulator layer front face, wiring can be completely covered with the 1st barrier layer and the 2nd barrier layer. Therefore, as well as the manufacture approach of the above 1st even if it forms wiring with copper or a copper alloy, migration of the copper under wiring, for example, the ionized copper, can be prevented. Therefore, the thing which has high wiring dependability and which suppressed short generating

during wiring and generating of leakage current can be manufactured.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] however, with the wiring structure explained by the Prior art Since there are few touch areas of the barrier metal layer formed in the inside of a wiring gutter and the nitride formed in the top face of copper wiring and the top face of copper wiring and the contact surface of a barrier metal layer and a nitride exist on the same flat surface mostly, For example, when a barrier metal layer and a nitride are removed by the stress of copper wiring, by it, the copper of copper wiring will move in the direction of the silicon oxide film from the interface of a barrier metal layer and a nitride. It is because it is the matter which copper tends [very] to move. It becomes the cause of leakage current, and that will cause a short circuit with adjoining copper wiring, when the worst.
[0014] Moreover, it is reported that the surface diffusion of copper of the interface and the various ingredients with which the laminating of two kinds of ingredients was carried out is very large. For example, in 1998 International Conference on SolidState Devices and Materials, S.U.Kim and others has reported the anomalous diffusion by which induction was carried out to the defect at the time of processing by the interface of BCB and a silicon nitride film. Thereby, in copper wiring, only thermal diffusion was understood that just minding is inadequate.

[Translation done.]

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MEANS

[Means for Solving the Problem] This inventions are the semiconductor device made in order to solve the above-mentioned technical problem, and its manufacture approach.
[0016] In the semiconductor device which equipped with wiring the interior of the crevice which formed the semiconductor device in the interlayer insulation film, it has the 1st barrier layer which covers the wiring concerned from the lower part side of wiring, and the 2nd barrier layer which covers the wiring concerned from the upper part side of wiring, the 1st barrier layer and the 2nd barrier layers overlap, and wiring is covered.
[0017] The 1st barrier layer which covers the wiring concerned with the above-mentioned semiconductor device from the lower part side of wiring, Since it has the 2nd barrier layer which covers the wiring concerned, the 1st barrier layer and the 2nd barrier layers overlap and wiring is covered from the upper part side of wiring, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer When the 1st barrier layer and the 2nd barrier layers overlap, even if one of barrier layers shift, the 1st barrier layer and the 2nd barrier layer hold contact in overlapping parts. That is, when the 1st barrier layer and the 2nd barrier layers overlap, a barrier layer comrade's adhesion force is strengthened. Therefore, the 1st barrier layer and the 2nd barrier layer separate, and the metal which constitutes wiring from the meantime does not move outside (or diffusion). Therefore, even if wiring is formed with copper or a copper alloy and the interlayer insulation film of silicon oxide is formed in the perimeter of wiring, the copper under wiring, for example, the ionized copper, does not move into an interlayer insulation film.
[0018] The process which forms wiring in the interior of a crevice by embedding a conductor while the manufacture approach of the 1st semiconductor device forms the 1st barrier layer in the inside of this crevice, after forming a crevice in an insulator layer, It is the manufacture approach equipped with the process which the insulator layer around wiring is removed [process] and makes wiring and the 1st barrier layer project from an insulator layer front face, and the process which overlaps the 1st barrier layer by the flank of wiring with a wrap in the upper part side of wiring, and forms the barrier layer of a wrap 2nd for wiring with the 1st barrier layer.
[0019] The process which forms wiring in the interior of a crevice by embedding a conductor while forming the 1st barrier layer in the inside of the crevice formed in the insulator layer by the manufacture approach of the 1st semiconductor device of the above, The process which the insulator layer around wiring is removed [process] and makes wiring and the 1st barrier layer project from an insulator layer front face, Since it has the process which overlaps the 1st barrier layer by the flank of wiring with a wrap in the upper part side of wiring, and forms the barrier layer of a wrap 2nd for wiring with the 1st barrier layer, wiring is covered with the 1st barrier layer and the 2nd barrier layer.
[0020] Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift when the 1st barrier layer and the 2nd barrier layers overlap, contact in the 1st barrier layer and the 2nd barrier layer will be maintained in overlapping parts. That is, a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer and the 2nd barrier layer may be overlapped. Therefore, since the 1st barrier layer and the 2nd barrier layer do not separate, the metal which a clearance opens in the meantime

and constitutes wiring does not move outside (or diffusion). Therefore, even if it forms wiring with copper or a copper alloy, the copper under wiring does not move into an insulator layer.
[0021] The process which forms wiring in the interior of a crevice by embedding a conductor while the manufacture approach of the 2nd semiconductor device forms the 1st barrier layer in the inside of this crevice, after forming a crevice in an insulator layer, It is the manufacture approach equipped with the process which removes the insulator layer near the top section of the 1st barrier layer, and forms a slot, and the process which forms the 2nd barrier layer in the condition of embedding a slot for the upper part side of wiring with a wrap.
[0022] The process which forms wiring in the interior of a crevice by embedding a conductor while forming the 1st barrier layer in the inside of the crevice formed in the insulator layer by the manufacture approach of the 2nd semiconductor device of the above, Since it has the process which removes the insulator layer near the top section of the 1st barrier layer, and forms a slot, and the process which forms the 2nd barrier layer in the condition of embedding a slot for the upper part side of wiring with a wrap, wiring is covered with the 1st barrier layer and the 2nd barrier layer.
[0023] Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift when the 1st barrier layer and the 2nd barrier layers overlap, contact in the 1st barrier layer and the 2nd barrier layer will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer and the 2nd barrier layer may be overlapped. Therefore, since the 1st barrier layer and the 2nd barrier layer do not separate, the metal which a clearance opens in the meantime and constitutes wiring does not move outside (or diffusion). Therefore, even if it forms wiring with copper or a copper alloy, the copper under wiring does not move into an insulator layer.
[0024] The process which forms wiring in the interior of a crevice by embedding a conductor while the manufacture approach of the 3rd semiconductor device forms the 1st barrier layer in the inside of this crevice, after forming a crevice in an insulator layer, It is the manufacture approach equipped with the process which removes the upper part of wiring so that it may become lower than an insulator layer front face, and the process which overlaps the 1st barrier layer in the top section of wiring with a wrap in the upper part side of wiring, and forms the barrier layer of a wrap 2nd for wiring with the 1st barrier layer.
[0025] The process which forms wiring in the interior of a crevice by embedding a conductor while forming the 1st barrier layer in the inside of the crevice formed in the insulator layer by the manufacture approach of the 3rd semiconductor device of the above, From having the process which removes the upper part of wiring so that it may become lower than an insulator layer front face, and the process which overlaps the 1st barrier layer in the top section of wiring with a wrap in the upper part side of wiring, and forms the barrier layer of a wrap 2nd for wiring with the 1st barrier layer Wiring is covered with the 1st barrier layer and the 2nd barrier layer.
[0026] Therefore, even if the stress of wiring is added to the 1st barrier layer and the 2nd barrier layer and one of barrier layers shift when the 1st barrier layer and the 2nd barrier layers overlap, contact in the 1st barrier layer and the 2nd barrier layer will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer and the 2nd barrier layer may be overlapped. Therefore, since the 1st barrier layer and the 2nd barrier layer do not separate, the metal which a clearance opens in the meantime and constitutes wiring does not move outside (or diffusion). Therefore, even if it forms wiring with copper or a copper alloy, the copper under wiring does not move into an insulator layer.
[0027]
[Embodiment of the Invention] The outline configuration sectional view of drawing 1 explains the gestalt of the 1st operation concerning the semiconductor device of this invention.
[0028] As shown in drawing 1 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. The above-mentioned interlayer insulation film 21 is formed with silicon oxide. It is formed in this wiring gutter 22 at the condition that wiring 24 projects from the top face of the above-mentioned

interlayer insulation film 21 through the 1st barrier layer 23. Thus, the 1st barrier layer 23 has covered the above-mentioned wiring 24 from the lower part side. The 1st barrier layer 23 is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. The above-mentioned wiring 24 is formed with copper or a copper alloy.
[0029] The 2nd barrier layer 25 which furthermore covers the above-mentioned wiring 24 from an upper part side is formed in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0030] In addition, although it does not carry out illustration, the above-mentioned interlayer insulation film 21 may cover semiconductor devices, such as a transistor, capacity, and resistance, and wiring which were formed, for example on the semi-conductor substrate, may be a thing for flattening, or may cover a wiring layer. That is, it is the interlayer insulation film used for the usual semiconductor device.
[0031] The 1st barrier layer 23 which covers this wiring 24 with the gestalt of implementation of the above 1st from the lower part side of wiring 24, It has the 2nd barrier layer 25 which covers this wiring 24 from the upper part side of the above-mentioned wiring 24. Since the 1st barrier layer 23 and the 2nd barrier layers 25 overlap by the flank of wiring 24 and wiring 24 is covered, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 When the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, even if one of barrier layers (for example, 2nd barrier layer 25) shift, the 1st barrier layer 23 and the 2nd barrier layer 25 hold contact in overlapping parts.
[0032] That is, when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, a barrier layer comrade's adhesion force is strengthened. Therefore, the 1st barrier layer 23 and the 2nd barrier layer 25 separate, and the metal which constitutes wiring 24 from the meantime does not move in the exterior of an interlayer insulation film 21, i.e., the direction, (or diffusion). That is, even if the stress of wiring 24 works, the condition of having covered wiring 24 with the 1st barrier layer 23 and the 2nd barrier layer 25 does not change. Therefore, the copper which constitutes wiring 24 ionizes, for example, and does not move into the interlayer insulation film 21 around wiring 24.

[0033] Next, the outline configuration sectional view of drawing 2 explains the gestalt of the 2nd operation concerning the semiconductor device of this invention. In addition, the same sign is given to the same component part as said drawing 1 in drawing 2 .
[0034] As shown in drawing 2 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. The above-mentioned interlayer insulation film 21 is formed with silicon oxide. Wiring 24 is formed in this wiring gutter 22 through the 1st barrier layer 23. Thus, the 1st barrier layer 23 has covered the above-mentioned wiring 24 from the lower part side. The 1st barrier layer 23 is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. The above-mentioned wiring 24 is formed with copper or a copper alloy.
[0035] The 2nd barrier layer 25 is formed so that a slot 26 may furthermore be formed in the interlayer insulation film 21 of the top section of the barrier layer 23 of the above 1st and the slot 26 may be embedded, and so that the above-mentioned wiring 24 may be covered from an upper part side. Thus, since the 2nd barrier layer 25 is formed, the 2nd barrier layer 25 is in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Or it is also possible to form by carbonization silicon, the tantalum, the tantalum alloy, tantalum nitride, etc. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0036] Since the 1st barrier layer 23 and the 2nd barrier layer 25 have covered wiring 24 with the gestalt of implementation of the above 2nd in the condition that the 1st barrier layer 23 and the 2nd barrier layers 25 overlap by the flank of wiring 24 It can prevent that the copper which constitutes wiring 24 ionizes the gestalt of said 1st operation, for example, and moves it into the

interlayer insulation film 21 around wiring 24 similarly in the 1st barrier layer 23 and the 2nd barrier layer 25.
[0037] Next, the outline configuration sectional view of drawing 3 explains the gestalt of the 3rd operation concerning the semiconductor device of this invention. In addition, the same sign is given to the same component part as said drawing 1 in drawing 3 .
[0038] As shown in drawing 3 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. The above-mentioned interlayer insulation film 21 is formed with silicon oxide. Wiring 24 is formed in this wiring gutter 22 through the 1st barrier layer 23. Thus, the 1st barrier layer 23 has covered the above-mentioned wiring 24 from the lower part side. The 1st barrier layer 23 is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. The above-mentioned wiring 24 is formed with copper or a copper alloy.
[0039] The 2nd barrier layer 27 is formed so that a slot 26 may furthermore be formed in the interlayer insulation film 21 near the top section of the barrier layer 23 of the above 1st and the slot 26 may be embedded, and so that the above-mentioned wiring 24 may be covered from an upper part side. Thus, since the 2nd barrier layer 27 is formed, the 2nd barrier layer 27 is in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 27 is formed by low dielectric constant organic film like for example, the aryl ether as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 27.
[0040] In addition, the low dielectric constant organic film can be used for the barrier layer of the above 2nd because the diffusion coefficient of the copper to the low dielectric constant organic film is small.
[0041] Since the 1st barrier layer 23 and the 2nd barrier layer 27 have covered wiring 24 with the gestalt of implementation of the above 3rd in the condition that the 1st barrier layer 23 and the 2nd barrier layers 27 overlap by the flank of wiring 24 It can prevent that the copper which constitutes wiring 24 ionizes the gestalt of said 1st operation, for example, and moves it into the interlayer insulation film 21 around wiring 24 similarly in the 1st barrier layer 23 and the 2nd barrier layer 27. Moreover, the 2nd barrier layer 27 can be used as an interlayer insulation film during wiring with wiring 24 and wiring (not shown) formed in the upper part.
[0042] Next, the outline configuration sectional view of drawing 4 explains the gestalt of the 4th operation concerning the semiconductor device of this invention. In addition, the same sign is given to the same component part as said drawing 1 in drawing 4 .
[0043] As shown in drawing 4 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. The above-mentioned interlayer insulation film 21 is formed with silicon oxide. The 1st barrier layer 23 is formed in the wall (a pars basilaris ossis occipitalis is also included) of this wiring gutter 22. The barrier layer 23 of the above 1st is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. Furthermore, it is formed in the above-mentioned wiring gutter 22 at the condition of having dented wiring 24 from the top face of the above-mentioned interlayer insulation film 21 through the barrier layer 23 of the above 1st. This wiring 24 is formed with copper or a copper alloy.
[0044] Therefore, the barrier layer 23 of the above 1st is formed also on the side of the above-mentioned wiring 24 in the above-mentioned wiring gutter 22, and the lower part side of the above-mentioned wiring 24 is covered with the 1st barrier layer 23.
[0045] The 2nd barrier layer 25 which furthermore covers the above-mentioned wiring 24 from an upper part side is formed in the condition of overlapping by the barrier layer 23 of the above 1st, and the side attachment wall of the above-mentioned wiring gutter 22. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.

[0046] In addition, although it does not carry out illustration, the above-mentioned interlayer insulation film 21 may cover semiconductor devices, such as a transistor, capacity, and

resistance, and wiring which were formed, for example on the semi-conductor substrate, may be a thing for flattening, or may cover a wiring layer. That is, it is the interlayer insulation film used for the usual semiconductor device.
[0047] The 1st barrier layer 23 which covers this wiring 24 with the gestalt of implementation of the above 4th from the lower part side of wiring 24, It has the 2nd barrier layer 25 which covers this wiring 24 from the upper part side of the above-mentioned wiring 24. Since the 1st barrier layer 23 and the 2nd barrier layers 25 overlap by the flank of a wiring gutter 22 and wiring 24 is covered, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 When the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, even if one of barrier layers (for example, 2nd barrier layer 25) shift, contact in the 1st barrier layer 23 and the 2nd barrier layer 25 will be held in overlapping parts.
[0048] That is, when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, a barrier layer comrade's adhesion force is strengthened. Therefore, the 1st barrier layer 23 and the 2nd barrier layer 25 separate, and the metal which constitutes wiring 24 from the meantime does not move in the exterior of an interlayer insulation film 21, i.e., the direction, (or diffusion). That is, even if the stress of wiring 24 works, the condition of having covered wiring 24 with the 1st barrier layer 23 and the 2nd barrier layer 25 does not change. Therefore, the copper which constitutes wiring 24 ionizes, for example, and does not move into the interlayer insulation film 21 around wiring 24.

[0049] Next, the production process Fig. of drawing 5 explains the gestalt of the operation concerning the 1st manufacture approach of this invention. The same sign is given to the component part which showed as an example the manufacture approach of the semiconductor device explained by said drawing 1 , and was shown by said drawing 1 , and the same components in drawing 5 .
[0050] As shown in (1) of drawing 5 , semiconductor devices (for example, a transistor, capacity, resistance, etc.) are formed in a semi-conductor substrate (illustration abbreviation), and lower layer wiring, a circuit pattern, etc. are further formed in it. On such a semi-conductor substrate, the wrap insulator layer 11 is formed in those components, wiring, etc. An interlayer insulation film 21 is formed on the insulator layer 11. This interlayer insulation film 21 is formed by the cascade screen of low dielectric constant organic film, such as for example, the aryl ether, and the silicon oxide film. Or it forms by the so-called low dielectric constant film, such as a cascade screen of the fluororesin film and the silicon oxide film, fluorine oxide-ized silicon film, organic SOG film, and inorganic SOG film. It is required for a design rule to contain the low dielectric constant film with the device after 0.13-micrometer generation especially.
[0051] then, DAMASHIN generally known -- after forming a crevice (it explains as a wiring gutter hereafter) 22 in an interlayer insulation film 21, the 1st barrier layer 23 is formed in the inside of a wiring gutter 22 by tantalum nitride or the tantalum by law as an ingredient which has barrier property to a copper atom and a copper ion. Furthermore, after forming a copper seed layer in the inside of a wiring gutter 22 through the 1st barrier layer 23, the interior of a wiring gutter 22 is embedded with a conductor (for example, copper) by the electrolysis galvanizing method etc. Then, for example by CMP, the excessive copper on an interlayer insulation film 21 and the 1st barrier layer 23 are removed, and the wiring 24 which becomes the interior of a wiring gutter 22 from copper through the 1st barrier layer 23 is formed.
[0052] Next, etching removes the interlayer insulation film 21 around wiring 24, and wiring 24 and the 1st barrier layer 23 are made to project from the front face of an interlayer insulation film 21, as shown in (2) of drawing 5 . Therefore, the 1st barrier layer 23 is in the condition of having covered the above-mentioned wiring 24 from the lower part side.
[0053] By the above-mentioned etching, when an interlayer insulation film 21 is silicon oxide film, wet etching removes here [the fluoric acid water solution and here] whose concentration is 0.1% - 1.0%, using 0.5% of fluoric acid water solution as an example. In addition, since an etching rate becomes late in the wet etching using the fluoric acid water solution of less than 0.1% of concentration, it is not practical, and since a metal part will also be etched in the wet etching using the fluoric acid water solution exceeding 1.0%, it is not desirable. Moreover, in the case of low dielectric constant organic film like the aryl ether, an interlayer insulation film 21 removes by

hydrogen plasma etching or nitrogen plasma etching. In addition, since the copper of wiring 24 is oxidized and it becomes a defect's cause, it is not desirable to use oxygen plasma etching. Moreover, it is desirable to perform from a viewpoint of antioxidizing of wiring 24 to formation of the 2nd barrier layer performed to this etching and degree by the non-oxidizing atmosphere. Namely, the so-called in situ Processing is desirable.

[0054] Moreover, it is also possible to perform etching of the above-mentioned interlayer insulation film 21 by the dry etching using the gas of a carbon fluoride system. In this case, the upper part of the 1st barrier layer 23 may also be etched. In addition, even if the upper part of the 1st barrier layer 23 is etched, it is necessary to perform the above-mentioned etching so that the amount of laps to the 1st barrier layer 23 of the 2nd barrier layer formed after that can fully secure, namely, so that it may leave the 1st barrier layer 23 to height of 30nm or more from the front face of the interlayer insulation film 21 after etching.

[0055] It is desirable to form the height of the level difference of an interlayer insulation film 21 and the 1st barrier layer 23 in at least 30nm or more by etching of the above-mentioned interlayer insulation film 21. It is because a lap part with the 2nd barrier layer formed behind decreases, it becomes difficult to secure sufficient barrier property and it becomes being the same as that of the structure of the conventional barrier layer, when the above-mentioned level difference is 30nm or less.

[0056] Next, as shown in (3) of drawing 5 , the 2nd barrier layer 25 is formed on the above-mentioned interlayer insulation film 21 so that the above-mentioned wiring 24 may be covered. This 2nd barrier layer 25 is formed by insulator layers, such as silicon nitride and hydrogenation silicon carbon, as an ingredient which has barrier property to a copper atom and a copper ion. As the manufacture approach, a CVD method is desirable. As the other membrane formation approaches, the membrane formation approaches, such as sputtering and a sol gel process, can also be used. When forming membranes with a CVD method, it is etching and in situ of the above-mentioned interlayer insulation film 21. Processing is desirable. for example, etching using the hydrogen plasma after etching the silicon oxide film in a rare fluoric acid water solution -- about [5nm-20nm] etching -- carrying out -- after that -- continuing -- chemical vapor growth (CVD [say / the following and CVD] is the abbreviation for Chemical Vapour Deposition) -- the 2nd barrier layer 25 which consists of a silicon nitride film by law is formed.

[0057] When an interlayer insulation film 21 is organic film, 10nm - about 100nm is etched by etching which used the hydrogen plasma or the nitrogen plasma, and the 2nd barrier layer 25 is formed with a silicon nitride film with a CVD method after that. As for a silicon nitride film, at this time, it is desirable to form in the thickness of 20nm - about 100nm. Barrier property sufficient in less than 20nm is not obtained. On the other hand by the thickness exceeding 100nm, the capacity between wiring becomes large, and it is not desirable. Thus, by etching using the hydrogen plasma, the oxide film (copper oxide film) of the front face of wiring 24 is etched, the front face of wiring 24 is cleaned to coincidence, and adhesion with the 2nd barrier layer 25 which consists of a silicon nitride film improves.

[0058] Moreover, in case the 2nd barrier layer 25 which consists of a silicon nitride film with a CVD method is formed, it is desirable to form so that the thickness of the side attachment wall of wiring 24 may become thin rather than the thickness on wiring 24. If a silicon nitride film is formed between wiring, since the capacity between wiring will rise, it is for controlling the rise of the capacity between wiring as much as possible. Therefore, it is good to form membranes in a CVD method, using high density plasma-CVD equipment as a CVD method which has directivity. Or it is good to form membranes using parallel monotonous mold plasma-CVD equipment. As the membrane formation condition, a step hippo ridge considers as the conditions used as about 30% or less. As membrane formation conditions at the time of using parallel monotonous mold plasma-CVD equipment, as an example, 1.03kPa(s) and membrane formation temperature are set as 400 degrees C, and a process gas ratio is set as about mono-silane [SiH4]:ammonia (NH3) =3:1 for the pressure of a membrane formation ambient atmosphere. Furthermore, it is desirable to perform plasma treatment which includes either [at least] the hydrogen plasma or the nitrogen plasma just before CVD. As membrane formation conditions at the time of using high density plasma-CVD equipment, as an example, 1Pa or less and membrane formation

temperature are set as 200 degrees C - 400 degrees C, and a process gas ratio is set as about mono-silane [SiH4]:nitrogen (N2) =3:1.5-5 for the pressure of a membrane formation ambient atmosphere.
[0059] If the 2nd barrier layer 25 is formed as mentioned above, the 2nd barrier layer 25 will overlap the 1st barrier layer 23 by the flank of wiring 24 with a wrap in the upper part side of wiring 24, and will cover wiring 24 with the 1st barrier layer 23.
[0060] Then, as shown in (4) of drawing 5 , an interlayer insulation film 31 is formed on the 2nd barrier layer 25. As for an interlayer insulation film 31, it is desirable to include the low dielectric constant film. Although the aryl ether was used in this invention, otherwise, it is possible to use organic [SOG], inorganic [SOG], a fluororesin, xerogel, etc.
[0061] In addition, although illustration is not carried out, the plug is formed in the location to a connection hole and its interior predetermined [of the above-mentioned insulator layer 11]. Moreover, in forming wiring 24 by the dual DAMASHIN method, in case a connection hole is formed in the position of the above-mentioned insulator layer 11 by the dual DAMASHIN method and it forms wiring 24, the conductor which forms wiring 24, for example, copper, is embedded, and a plug is formed also in the interior of a connection hole.
[0062] By the 1st manufacture approach explained by above-mentioned drawing 5 After forming in the interior of a wiring gutter 22 the wiring 24 which consists of copper through the 1st barrier layer 23, the interlayer insulation film 21 around wiring 24 is removed. Wiring 24 and the 1st barrier layer 23 are made to project from the front face of an interlayer insulation film 21. Then, since the 1st barrier layer 23 is overlapped by the flank of wiring 24 with a wrap in the upper part side of wiring 24 and the barrier layer 25 of a wrap 2nd is formed for wiring 24 with the 1st barrier layer 23, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0063] Therefore, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 and one of barrier layers shift when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, contact in the 1st barrier layer 23 and the 2nd barrier layer 25 will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer 23 and the 2nd barrier layer 25 may be overlapped. Therefore, since the 1st barrier layer 23 and the 2nd barrier layer 25 do not separate, the copper which a clearance opens in the meantime and constitutes wiring 24 does not move outside (or diffusion). Therefore, even if it forms wiring 24 with copper (or copper alloy) as mentioned above and uses the silicon oxide film for the above-mentioned interlayer insulation film 21, the copper under wiring 24, for example, the ionized copper, does not move into an interlayer insulation film 21.
[0064] Moreover, in the manufacture approach of the above 1st, the interlayer insulation film 21 has a laminated structure of the low dielectric constant organic film and the silicon oxide film. The upper part of an interlayer insulation film 21 is formed by the silicon oxide film, and when the thickness of the silicon oxide film is 30nm - about 100nm In order to make wiring 24 and the 1st barrier layer 23 project, in the process which removes the upper part of an interlayer insulation film 21, all the silicon oxide film parts of an interlayer insulation film 21 may be removed.
[0065] Next, the production process Fig. of drawing 6 explains the gestalt of the 1st operation concerning the 2nd manufacture approach of this invention. The same sign is given to the component part which showed as an example the manufacture approach of the semiconductor device explained by said drawing 2 , and was shown by said drawing 2 , and the same components in drawing 6 .
[0066] the approach same as shown in (1) of drawing 6 , i.e., DAMASHIN generally known, as (1) of said drawing 5 explained -- after forming a crevice (it explains as a wiring gutter hereafter) 22 in an interlayer insulation film 21, the 1st barrier layer 23 is formed in the inside of a wiring gutter 22 by tantalum nitride or the tantalum by law as an ingredient which has barrier property to a copper atom and a copper ion. Furthermore, after forming a copper seed layer in the inside of a wiring gutter 22 through the 1st barrier layer 23, the interior of a wiring gutter 22 is embedded with a conductor (for example, copper) by the electrolysis galvanizing method etc. Then, for example by CMP, the excessive copper on an interlayer insulation film 21 and the 1st barrier layer 23 are removed, and the wiring 24 which becomes the interior of a wiring gutter 22

from copper through the 1st barrier layer 23 is formed.
[0067] Subsequently, as shown in (2) of drawing 6 , an interlayer insulation film 21 is etched. Conditions into which the interlayer insulation film 21 in the side periphery of the 1st barrier layer 23 is etched in the etching conditions in that case are chosen. In for example, the case of the silicon oxide film with which an interlayer insulation film 21 contains 10% - 20% of carbon a magnetron mold etching system -- using -- etching gas -- an argon [trifluoromethane / (CHF3) / [a supply flow rate is set for example, to 5sccm(s)]] -- an oxygen (O2) [supply flow rate is set [(Ar / [a supply flow rate is set) for example, to 20sccm(s)]] for example, to 5sccm (s) --] -- using -- What is necessary is to set the pressure of an etching ambient atmosphere as 5Pa, to set impression power as 600W, and just to carry out whole surface etchback of the interlayer insulation film 21 as an example. A slot 26 is formed in the interlayer insulation film 21 near the top section of the barrier layer 23 of the above 1st by carrying out etchback on such conditions.
[0068] Then, as shown in (3) of drawing 6 , the 2nd barrier layer 25 is formed so that the above-mentioned slot 26 may be embedded, and so that the above-mentioned wiring 24 may be covered from an upper part side. Thus, since the 2nd barrier layer 25 is formed, the 2nd barrier layer 25 will be in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0069] With the gestalt of the 1st operation concerning the 2nd manufacture approach explained by above-mentioned drawing 6 Wiring 24 is formed in the interior of the wiring gutter 22 formed in the interlayer insulation film 21 through the 1st barrier layer 23. Subsequently, since the 2nd barrier layer 25 is formed in the condition of embedding a slot 26 for the upper part side of wiring 24 with a wrap after removing the interlayer insulation film 21 near the top section of the 1st barrier layer 23 and forming a slot 26, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0070] Therefore, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 and one of barrier layers shift when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, contact in the 1st barrier layer 23 and the 2nd barrier layer 25 will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer 23 and the 2nd barrier layer 25 may be overlapped. Therefore, since the 1st barrier layer 23 and the 2nd barrier layer 25 do not separate, the copper which a clearance opens in the meantime and constitutes wiring 24 does not move outside (or diffusion). Therefore, even if it forms wiring 24 with copper (or copper alloy) as mentioned above and uses the silicon oxide film for the above-mentioned interlayer insulation film 21, the copper under wiring 24, for example, the ionized copper, does not move into an interlayer insulation film 21.
[0071] Next, the production process Fig. of drawing 7 explains the gestalt of the 2nd operation concerning the 2nd manufacture approach of this invention. The same sign is given to the component part which showed as an example the manufacture approach of the semiconductor device explained by said drawing 3 , and was shown by said drawing 3 , and the same components in drawing 7 .
[0072] By the same approach, a crevice (it explains as a wiring gutter hereafter) 22 is formed in an interlayer insulation film 21, and the wiring 24 which becomes the interior of the wiring gutter 22 from copper through the 1st barrier layer 23 is formed as (1) of said drawing 6 and (2) explained. Subsequently, etchback of the interlayer insulation film 21 is carried out, and a slot 26 is formed in the interlayer insulation film 21 of the top section of the barrier layer 23 of the above 1st.
[0073] Then, as are shown in drawing 7 , and the above-mentioned wiring 24 is covered from an upper part side so that the above-mentioned slot 26 may be embedded and, the 2nd barrier layer 27 is formed on an interlayer insulation film 21. This 2nd barrier layer 27 is formed by low dielectric constant organic film like for example, the aryl ether as an ingredient which has barrier property to a copper atom and a copper ion. Thus, the 2nd barrier layer 27 is formed in the

condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24.
[0074] Therefore, the same operation effectiveness as the gestalt of implementation of the above 1st is acquired. That is, since wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 17 even if it forms wiring 24 with copper (or copper alloy) as mentioned above and therefore uses the silicon oxide film for the above-mentioned interlayer insulation film 21, the copper under wiring 24, for example, the ionized copper, does not move into an interlayer insulation film 21.
[0075] Next, the production process Fig. of drawing 8 explains the gestalt of the operation concerning the 3rd manufacture approach of this invention. The same sign is given to the component part which showed as an example the manufacture approach of the semiconductor device explained by said drawing 4 , and was shown by said drawing 4 , and the same components in drawing 8 .
[0076] As shown in (1) of drawing 8 , semiconductor devices (for example, a transistor, capacity, resistance, etc.) are formed in a semi-conductor substrate (illustration abbreviation), and lower layer wiring, a circuit pattern, etc. are further formed in it. On such a semi-conductor substrate, the wrap insulator layer 11 is formed in those components, wiring, etc. An interlayer insulation film 21 is formed on the insulator layer 11. This interlayer insulation film 21 is formed by the cascade screen of organic film, such as for example, the aryl ether, and the silicon oxide film. Or it forms by the so-called low dielectric constant film, such as a cascade screen of the fluororesin film and the silicon oxide film, fluorine oxide-ized silicon film, organic SOG film, and inorganic SOG film. It is required for a design rule to contain the low dielectric constant film with the device after 0.13-micrometer generation especially.
[0077] then, DAMASHIN generally known -- after forming a crevice (it explains as a slot below) in an interlayer insulation film 21, the 1st barrier layer 23 is formed in the inside of a wiring gutter 22 by tantalum nitride or the tantalum by law as an ingredient which has barrier property to a copper atom and a copper ion. Furthermore, after forming a copper seed layer in the inside of a wiring gutter 22 through the 1st barrier layer 23, the interior of a wiring gutter 22 is embedded with a conductor (for example, copper) by the electrolysis galvanizing method etc. Then, for example by CMP, the excessive copper on an interlayer insulation film 21 and the 1st barrier layer 23 are removed, and the wiring 24 which becomes the interior of a wiring gutter 22 from copper through the 1st barrier layer 23 is formed.
[0078] Next, as shown in (2) of drawing 8 , only the upper part where the top face of wiring 24 becomes low rather than the front face of an interlayer insulation film 21 and which is wiring 24 that it will be is etched alternatively. It is desirable to form the height of the level difference of wiring 24 and the 1st barrier layer 23 in at least 30nm or more by the above-mentioned etching. It is because a lap part with the 2nd barrier layer formed behind decreases, it becomes difficult to secure sufficient barrier property and it becomes being the same as that of the structure of the conventional barrier layer, when the above-mentioned level difference is 30nm or less.
[0079] Subsequently, as shown in (3) of drawing 8 , sputter etching or hydrogen plasma etching removes the front face of wiring 24 for an oxide film etc. Then, for example by sputtering, the 2nd barrier layer 25 is formed on an interlayer insulation film 21 so that wiring 24 may be covered. The barrier layer 25 of the above 2nd is formed by the tantalum, tantalum nitride, etc. as an ingredient which has barrier property to a copper atom and a copper ion. As the other membrane formation approaches, it is also possible to use the membrane formation approaches, such as a steamy method and a CVD method.
[0080] In addition, in order not to make the front face of wiring 24 generate an oxide film, it is desirable to perform the period until it forms the 2nd barrier layer 25 from the above-mentioned sputter etching or hydrogen plasma etching by the non-oxidizing atmosphere. For example, the so-called in situ Processing is desirable. For example, by sputter etching, 5nm - about 20nm is etched, and the 2nd barrier layer 25 which consists of tantalum film by sputtering continuously is formed after that. As for this tantalum film, it is desirable to form in the thickness of 20nm - about 75nm. Barrier property sufficient in less than 20nm is not obtained. On the other hand, by the thickness exceeding 75nm, processing will take time amount and wiring resistance will

become large too much.
[0081] Then, as shown in (4) of drawing 8 , CMP removes the 2nd barrier layer 25 on an interlayer insulation film 21. Consequently, the configuration whose 1st barrier layer 23 and 2nd barrier layer 25 overlap in the top section of wiring 24, and cover wiring 24 with the 1st barrier layer 23 and the 2nd barrier layer 25 in a wiring gutter 22 is completed. Thus, since the 2nd barrier layer 25 on an interlayer insulation film 21 is removed, it becomes possible to form the 2nd barrier layer 25 by the tantalum nitride and the tantalum of a conductor.
[0082] Then, although illustration is not carried out, an interlayer insulation film 31 is formed on the 2nd barrier layer 25 and an interlayer insulation film 21 like said 1st manufacture approach. As for an interlayer insulation film 31, it is desirable to include the low dielectric constant film. Although the aryl ether was used in this invention, otherwise, it is possible to use organic [SOG], inorganic [SOG], a fluororesin, xerogel, etc.
[0083] In addition, it is also possible to form the barrier layer 25 of the above 2nd by insulator layers, such as a silicon nitride film explained by said 1st manufacture approach and hydrogenation silicon carbon. The membrane formation approach in that case, membrane formation conditions, etc. are the same with having explained by the 1st manufacture approach.
[0084] Moreover, in the manufacture approach of the above 3rd, although illustration is not carried out, the plug is formed in the location to a connection hole and its interior predetermined [of the above-mentioned insulator layer 11]. Moreover, in forming wiring 24 by the dual DAMASHIN method, in case a connection hole is formed in the position of the above-mentioned insulator layer 11 by the dual DAMASHIN method and it forms wiring 24, the conductor which forms wiring 24, for example, copper, is embedded, and a plug is formed also in the interior of a connection hole.
[0085] By the 2nd manufacture approach explained by above-mentioned drawing 8 After forming in the interior of a wiring gutter 22 the wiring 24 which consists of copper through the 1st barrier layer 23, the upper part of wiring 24 is removed. Make the top face of wiring 24 lower than the front face of an interlayer insulation film 21, overlap the 1st barrier layer 23 by the flank of wiring 24 with a wrap in the upper part side of wiring 24 after that, and wiring 24 from forming the barrier layer 25 of a wrap 2nd with the 1st barrier layer 23 Wiring 24 comes to be covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0086] Therefore, even if the stress of wiring 24 is added to the 1st barrier layer 23 and the 2nd barrier layer 25 and one of barrier layers shift when the 1st barrier layer 23 and the 2nd barrier layers 25 overlap, contact in the 1st barrier layer 23 and the 2nd barrier layer 25 will be maintained in overlapping parts. That is, it is because a barrier layer comrade's adhesion force is strengthened by forming so that the 1st barrier layer 23 and the 2nd barrier layer 25 may be overlapped. Therefore, since the 1st barrier layer 23 and the 2nd barrier layer 25 do not separate, the copper which a clearance opens in the meantime and constitutes wiring 24 does not move outside (or diffusion). Therefore, even if it forms wiring 24 with copper (or copper alloy) as mentioned above and uses the silicon oxide film for the above-mentioned interlayer insulation film 21, the copper under wiring 24, for example, the ionized copper, does not move into an interlayer insulation film 21.
[0087] In addition, it is also possible to consider as the structure concerning the semiconductor device of this invention as shown in drawing 9 as a gestalt of the 5th operation. It is explained below.
[0088] As shown in drawing 9 , the crevice (it explains as a wiring gutter hereafter) 22 is formed in the interlayer insulation film 21 which constitutes some semiconductor devices. It is formed in this wiring gutter 22 at the condition that wiring 24 projects from the top face of the above-mentioned interlayer insulation film 21 through the 1st barrier layer 23. And the 1st barrier layer 23 is formed also on the interlayer insulation film 21 around a wiring gutter 22. Thus, in order to form, after removing the conductor (for example, copper) for forming wiring deposited on the 1st barrier layer 23 in CMP, it is necessary to carry out patterning of the 1st barrier layer 23 according to the so-called mask process (a lithography technique and etching). In addition, the barrier layer 23 of the above 1st is formed by tantalum nitride or the tantalum as an ingredient which has barrier property to a copper atom and a copper ion. The above-mentioned wiring 24 is

formed with copper or a copper alloy.
[0089] The 2nd barrier layer 25 which furthermore covers the above-mentioned wiring 24 from an upper part side is formed in the condition of overlapping the barrier layer 23 of the above 1st by the flank (side face) of the above-mentioned wiring 24. This 2nd barrier layer 25 is formed with silicon nitride as an ingredient which has barrier property to a copper atom and a copper ion. Thus, wiring 24 is covered with the 1st barrier layer 23 and the 2nd barrier layer 25.
[0090] Also with the gestalt of implementation of the above 5th, the same effectiveness as said 1st explained operation gestalt is acquired.
[0091] When the lap width of face in the lengthwise direction of a wiring cross section with the 1st barrier layer 23, the 2nd barrier layer 25, or the 2nd barrier layer 27 explained with the gestalt of each above-mentioned implementation was required however had the thickness in the side face of the wiring 24 of the 1st barrier layer 23, or the side face of a wiring gutter 22, and more than comparable [about 45nm / a maximum of], it came out enough and a certain thing was checked by experiment of an artificer.
[0092] The 1st barrier layer 23 and the 2nd barrier layer 25, or the 2nd barrier layer 27 explained with the gestalt of each above-mentioned implementation can be applied also to a dual pellet syn conformation.
[0093] Moreover, even if it is the configuration which made vertical reverse the configuration explained with the gestalt of each above-mentioned implementation, it enters under the category of this invention.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the outline configuration sectional view concerning the semiconductor device of this invention showing the gestalt of the 1st operation.
[Drawing 2] It is the outline configuration sectional view concerning the semiconductor device of this invention showing the gestalt of the 2nd operation.
[Drawing 3] It is the outline configuration sectional view concerning the semiconductor device of this invention showing the gestalt of the 3rd operation.
[Drawing 4] It is the outline configuration sectional view concerning the semiconductor device of this invention showing the gestalt of the 4th operation.
[Drawing 5] It is the production process Fig. showing the gestalt of the operation concerning the 1st manufacture approach of this invention.
[Drawing 6] It is the production process Fig. concerning the 2nd manufacture approach of this invention showing the gestalt of the 1st operation.
[Drawing 7] It is the production process Fig. concerning the 2nd manufacture approach of this invention showing the gestalt of the 2nd operation.
[Drawing 8] It is the production process Fig. showing the gestalt of the operation concerning the 3rd manufacture approach of this invention.
[Drawing 9] It is the outline configuration sectional view concerning the semiconductor device of this invention showing the gestalt of the 5th operation.
[Drawing 10] It is a production process Fig. explaining the formation approach of wiring by the conventional DAMASHIN method.
[Description of Notations]
21 [-- Wiring, 25 / -- 2nd barrier layer] -- An interlayer insulation film, 22 -- A crevice (wiring gutter), 23 -- The 1st barrier layer, 24

[Translation done.]

* NOTICES *

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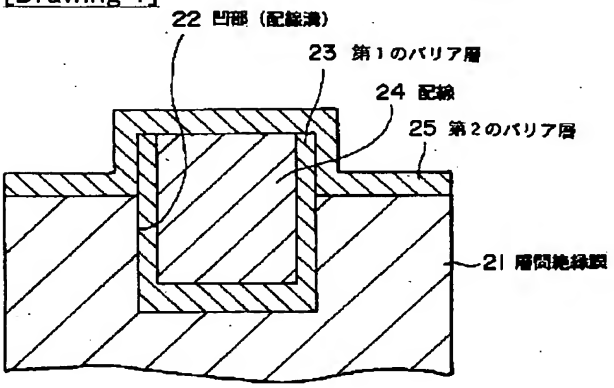
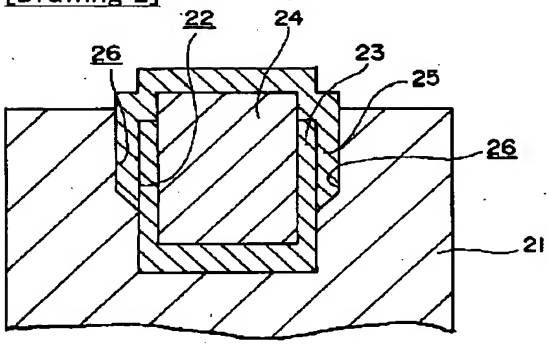
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

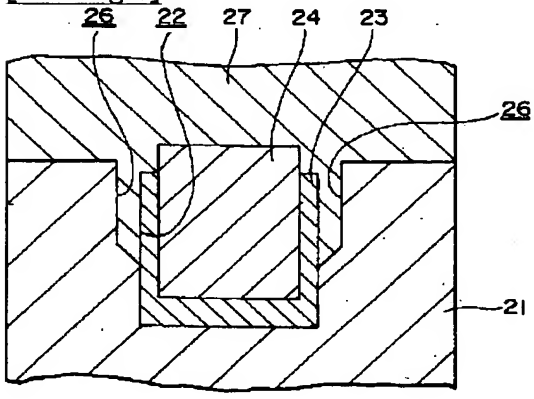
[Drawing 1]



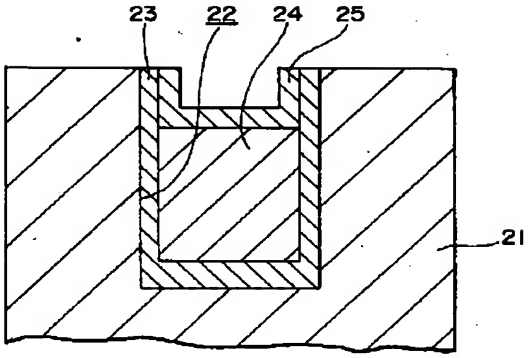
[Drawing 2]



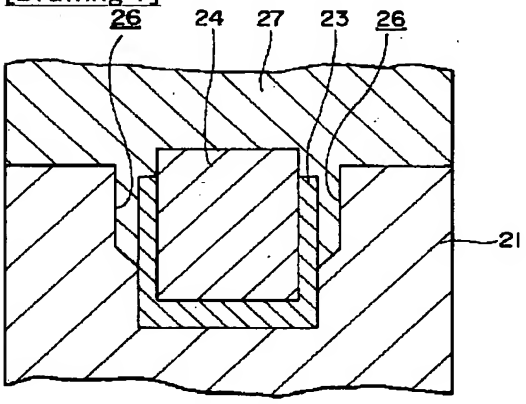
[Drawing 3]



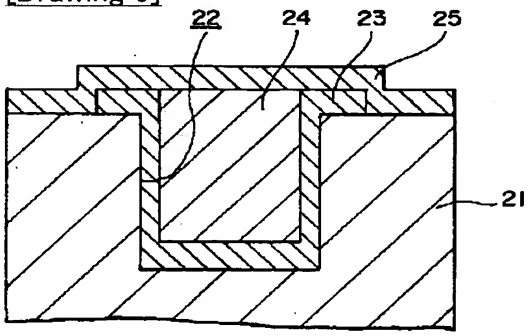
[Drawing 4]



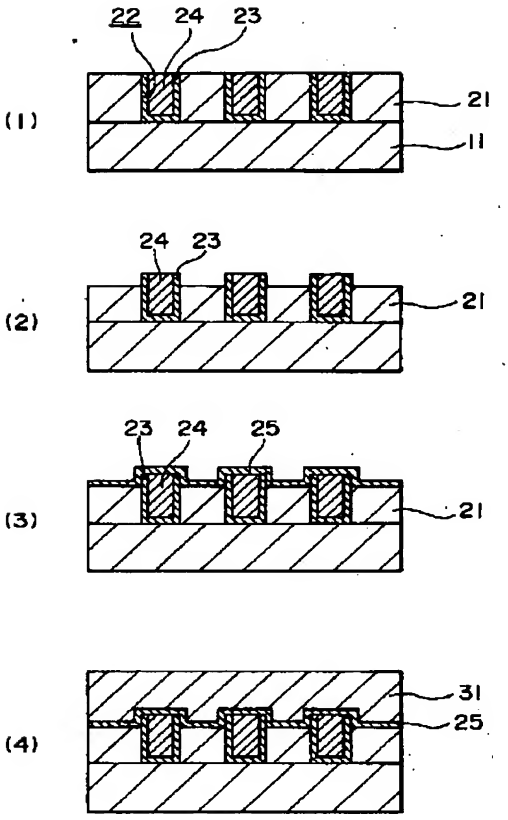
[Drawing 7]



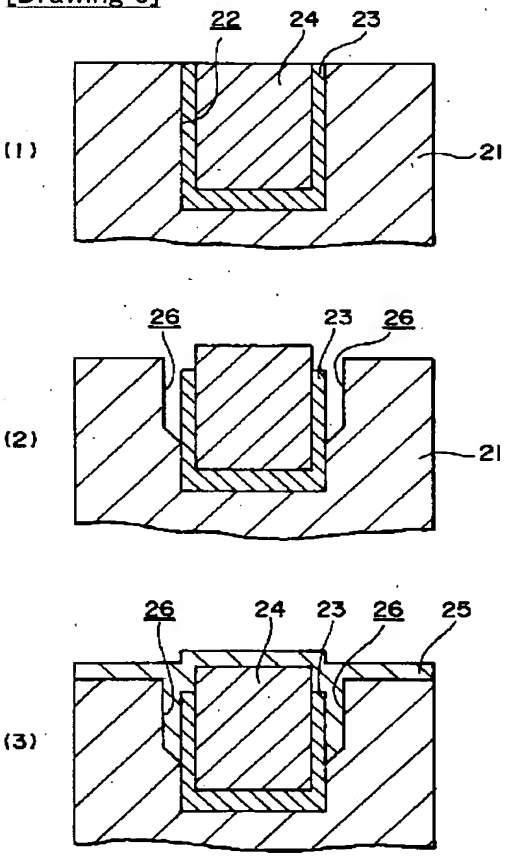
[Drawing 9]



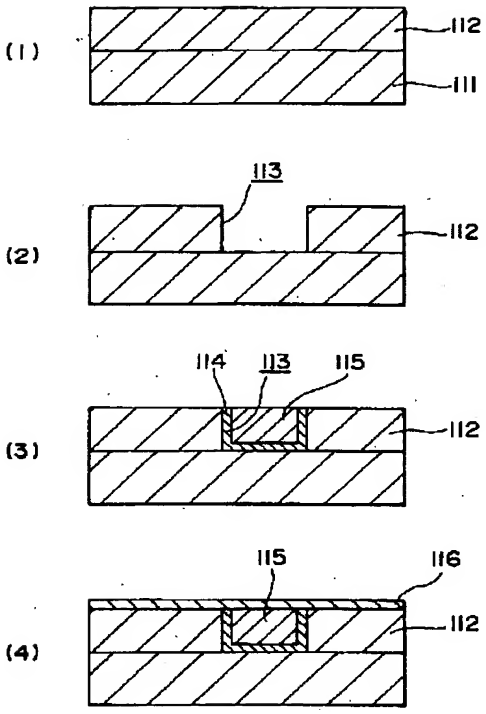
[Drawing 5]



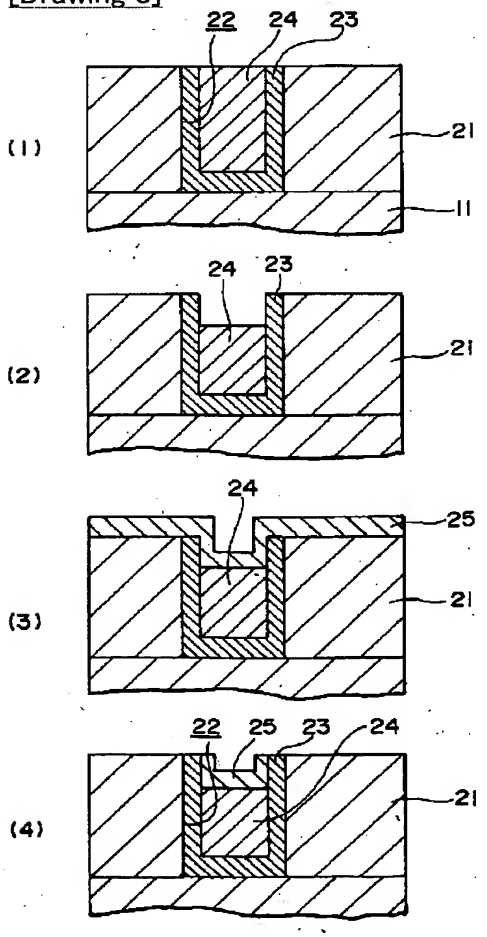
[Drawing 6]



[Drawing 10]



[Drawing 8]



[Translation done.]

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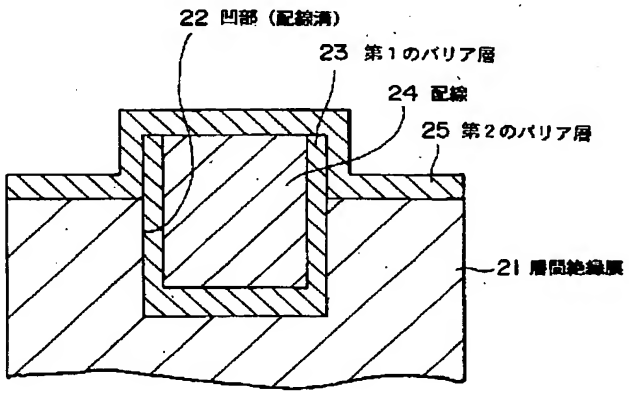
最終頁に続く

(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【課題】　配線溝の内部にバリアメタル層を介して形成した銅配線の上面に窒化膜を単に被覆した構成では、バリアメタル層と窒化膜との界面より層間絶縁膜方向に移動しようとする銅配線中の銅の移動を阻止し、リーク電流を発生および隣接する銅配線との短絡を防止する。
【解決手段】　層間絶縁膜２１に形成した凹部（配線溝）２２の内部に配線２４を形成した半導体装置において、配線２４の下部側より当該配線２４を被覆する第１のバリア層２３と、配線２４の上部側より当該配線２４を被覆する第２のバリア層２５とを備え、第１のバリア層２３と第２のバリア層２５とが重なりあって配線２４が被覆されているものである。



【特許請求の範囲】

【請求項１】　層間絶縁膜に形成した凹部の内部に配線を備えた半導体装置において、
前記配線の下部側より当該配線を被覆する第１のバリア層と、
前記配線の上部側より当該配線を被覆する第２のバリア層とを備え、
前記第１のバリア層と前記第２のバリア層とが重なりあって前記配線が被覆されていることを特徴とする半導体装置。

【請求項２】　前記第１のバリア層と前記第２のバリア層との重なり合っている部分は、前記配線の側部に設けられている、
ことを特徴とする請求項１記載の半導体装置。

【請求項３】　前記第１のバリア層と前記第２のバリア層との重なり合っている部分は、前記配線の上側部に設けられていることを特徴とする請求項１記載の半導体装置。

【請求項４】　前記凹部は、溝、もしくは接続孔、もしくは溝と該溝の底部に形成した接続孔とからなることを特徴とする請求項１記載の半導体装置。

【請求項５】　絶縁膜に凹部を形成した後、前記凹部の内面に第１のバリア層を形成するとともに前記凹部の内部に導電体を埋め込むことで配線を形成する工程と、
前記配線の周囲の前記絶縁膜を除去して、前記絶縁膜表面より前記配線と前記第１のバリア層とを突出させる工程と、
前記配線の上部側を覆うとともに前記配線の側部で前記第１のバリア層と重なり合って前記配線を前記第１バリア層とともに覆う第２のバリア層を形成する工程とを備えたことを特徴とする半導体装置の製造方法。

【請求項６】　前記配線の周囲の前記絶縁膜を除去する工程から前記第２のバリア層を形成する工程までを非酸化性雰囲気で行うことを特徴とする請求項５記載の半導体装置の製造方法。

【請求項７】　前記凹部は、溝、もしくは接続孔、もしくは溝と該溝の底部に形成した接続孔で形成されることを特徴とする請求項５記載の半導体装置の製造方法。

【請求項８】　絶縁膜に凹部を形成した後、前記凹部の内面に第１のバリア層を形成するとともに前記凹部の内部に導電体を埋め込むことで配線を形成する工程と、
前記第１のバリア層の上側部近傍の前記絶縁膜を除去して溝を形成する工程と、
前記配線の上部側を覆うとともに前記溝を埋め込む状態に第２のバリア層を形成する工程とを備えたことを特徴とする半導体装置の製造方法。

【請求項９】　前記配線の周囲の前記絶縁膜を除去する工程から前記第２のバリア層を形成する工程までを非酸化性雰囲気で行うことを特徴とする請求項８記載の半導体装置の製造方法。

【請求項１０】　前記凹部は、溝、もしくは接続孔、もしくは溝と該溝の底部に形成した接続孔で形成されることを特徴とする請求項８記載の半導体装置の製造方法。

【請求項１１】　絶縁膜に凹部を形成した後、前記凹部の内面に第１のバリア層を形成するとともに前記凹部の内部に導電体を埋め込むことで配線を形成する工程と、
前記絶縁膜表面よりも低くなるように前記配線の上部を除去する工程と、
前記配線の上部側を覆うとともに前記配線の上側部で前記第１のバリア層と重なり合って前記配線を前記第１バリア層とともに覆う第２のバリア層を形成する工程とを備えたことを特徴とする半導体装置の製造方法。

【請求項１２】　前記配線の上部を除去する工程から前記第２のバリア層を形成する工程までを非酸化性雰囲気で行うことを特徴とする請求項１１記載の半導体装置の製造方法。

【請求項１３】　前記凹部は、溝、もしくは接続孔、もしくは溝と該溝の底部に形成した接続孔で形成されることを特徴とする請求項１１記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、半導体装置およびその製造方法に関し、詳しくは銅もしくは銅合金を導電体に用いた半導体装置およびその製造方法に関する。

【０００２】

【従来の技術】半導体装置の微細化にともなって、配線の微細化、配線ピッチの縮小化が必要になっている。また同時に、低消費電力化および高速化などの要求にともない、層間絶縁膜の低誘電率化および配線の低抵抗化が必要になってきた。特にロジックデバイスでは、微細配線による抵抗上昇、配線容量の増加がデバイスの動作速度の低下につながるため、低誘電率膜を層間絶縁膜を用いた微細化された多層配線が必要になっている。

【０００３】配線幅の微細化、ピッチの縮小化は、配線自体の縦横比を大きくするだけではなく、配線間の間隔（ライン・アンド・スペースのスペース部分）のアスペクト比を大きくし、結果として、縦に細長い微細配線を形成する技術、微細な配線間を層間絶縁膜で埋め込む技術などに負担がかかり、プロセスを複雑にすると同時に、プロセス数の増大を招いている。

【０００４】接続孔（例えばビアホール）と配線溝とを金属（アルミニウム、銅等）のリフロースパッタリングもしくはメッキで同時に埋め込み、化学的機械研磨（以下ＣＭＰという）により表面の金属を研磨するダマシンプロセスでは、高アスペクト比の金属配線をエッチングで形成することも、配線間の挟隙を層間絶縁膜で埋め込む必要もなく、大幅にプロセス数を減らすことが可能である。このプロセスは、配線のアスペクト比が高くなるほど、配線総数が増大するほど、総製造コストの削減に

大きく寄与するようになる。

【０００５】従来、ＬＳＩの配線では、導電材料にアルミニウムおよびアルミニウム合金が用いられてきたが、近年、半導体集積回路の集積度の向上にともない、高速化、低消費電力化を達成するために、導電材料には銅合金が用いられるようになってきた。また、銅を配線材料に用いる製造方法は、従来のエッチングにより配線材料を加工した後に絶縁膜を被覆させるのではなく、先に絶縁膜を形成した後に、その一部に導電体を埋め込むための溝および孔を形成し、そのなかに導電体からなる配線材料を埋め込むダマシン法が開発されている。

【０００６】次に、ダマシン法による配線の形成方法を、図１０の製造工程により説明する。

【０００７】図１０の（１）に示すように、第１の絶縁層１１１上に第２の絶縁層１１２を形成する。第１の絶縁層１１１と第２の絶縁層１１２とは異なる絶縁材料で形成されたものであっても、同一絶縁材料で形成されたものであってもよい。

【０００８】次に、図１０の（２）に示すように、通常のリソグラフィー技術とエッチング技術とによって、第２の絶縁層１１２に配線または電極を形成するための溝１１３を形成する。

【０００９】続いて、図１０の（３）に示すように、この上記溝１１３の内面にバリアメタル層１１４を形成し、さらに導電体として銅を埋め込む。その後、溝１１３からはみ出したバリアメタル層１１４と銅とを、化学的機械研磨（以下ＣＭＰという、ＣＭＰはChemical Mechanical Polishing の略）法により、除去し、その表面を平坦化する。このようにして、溝１１３の内部にバリアメタル層１１４を介して銅からなる配線１１５を形成する。この図では、バリアメタル層１１４は、第１の絶縁層１１１および第２の絶縁層１１２への拡散（移動）を防止するためのものであり、現在はタンタルもしくはタンタル化合物もしくはタンタル合金が用いられることが多い。その他の材料では、チタン、チタン合金、タングステン等が用いられている。

【００１０】その後、図１０の（４）に示すように、配線１１５の上部を被覆するように、第２の絶縁層１１２上に窒化膜（例えば窒化シリコン膜）１１６を形成する。この窒化膜１１６は配線１１５中の銅の上部への拡散を防止するためのものである。

【００１１】上記図１０では、溝１１３中に銅からなる配線１１５を形成した場合を示したが、下層配線との接続孔を上層配線を埋め込む溝と同時に形成し、その溝と接続孔とに同時に導電体を埋め込むデュアルダマシン法でも、溝内に形成されるバリアメタル層と配線上に形成される窒化膜とは同様なる構成を有している。

【００１２】一方、銅を導電材料にするための問題点が指摘されている。すなわち、銅はアルミニウムのように種々の材料と容易に酸化物を形成する材料ではないので、層間絶縁膜および配線間絶縁膜中を容易に移動（拡散）する。したがって、半導体装置において、銅配線を実現するためには、銅の移動を阻止するいわゆるバリア層の形成が必須技術になる。そのため、バリア層によって、確実に銅の移動を阻止する必要がある。

【００１３】

【発明が解決しようとする課題】しかしながら、従来の技術で説明した配線構造では、配線溝の内面に形成したバリアメタル層と銅配線の上面に形成した窒化膜との接触面積が少なく、また銅配線の上面と、バリアメタル層と窒化膜との接触面とがほぼ同一平面上に存在しているため、例えば銅配線のストレスによって、バリアメタル層と窒化膜とが剥がされた場合には、銅配線の銅がバリアメタル層と窒化膜との界面より酸化シリコン膜方向に移動してしまう。それは、銅が非常に移動し易い物質であるためである。そのことが、リーク電流の原因になり、最悪の場合には隣接する銅配線との短絡を引き起こすことになる。

【００１４】また、銅は、２種類の材料が積層された界面や各種材料の表面拡散が非常に大きいことが報告されている。例えば、1998 International Conference on SolidState Devices and Materialsにおいて、Ｓ．Ｕ．ＫｉｍらがＢＣＢと窒化シリコン膜との界面での加工時の欠陥に誘起された異常拡散を報告している。これにより、銅配線では、熱拡散だけを留意するだけでは不十分であることがわかった。

【００１５】

【課題を解決するための手段】本発明は、上記課題を解決するためになされた半導体装置およびその製造方法である。

【００１６】半導体装置は、層間絶縁膜に形成した凹部の内部に配線を備えた半導体装置において、配線の下部側より当該配線を被覆する第１のバリア層と、配線の上部側より当該配線を被覆する第２のバリア層とを備え、第１のバリア層と第２のバリア層とが重なりあって配線が被覆されているものである。

【００１７】上記半導体装置では、配線の下部側より当該配線を被覆する第１のバリア層と、配線の上部側より当該配線を被覆する第２のバリア層とを備え、第１のバリア層と第２のバリア層とが重なりあって配線が被覆されていることから、配線のストレスが第１のバリア層および第２のバリア層に加えられても、第１のバリア層と第２のバリア層とが重なり合っていることにより、たとえ、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層と第２のバリア層とは接触を保持している。すなわち、第１のバリア層と第２のバリア層とが重なり合うことにより、バリア層同志の密着力が強化されている。そのため、第１のバリア層と第２のバリア層とが離れて、その間から配線を構成する金属が外部に移動（もしくは拡散）することがない。したが

って、配線が銅もしくは銅合金で形成され、配線の周囲に酸化シリコンの層間絶縁膜が形成されていても、配線中の銅、例えばイオン化した銅が層間絶縁膜中に移動することがない。

【００１８】第１の半導体装置の製造方法は、絶縁膜に凹部を形成した後、この凹部の内面に第１のバリア層を形成するとともに凹部の内部に導電体を埋め込むことで配線を形成する工程と、配線の周囲の絶縁膜を除去して、絶縁膜表面より配線と第１のバリア層とを突出させる工程と、配線の上部側を覆うとともに配線の側部で第１のバリア層と重なり合って配線を第１バリア層とともに覆う第２のバリア層を形成する工程とを備えた製造方法である。

【００１９】上記第１の半導体装置の製造方法では、絶縁膜に形成した凹部の内面に第１のバリア層を形成するとともに凹部の内部に導電体を埋め込むことで配線を形成する工程と、配線の周囲の絶縁膜を除去して、絶縁膜表面より配線と第１のバリア層とを突出させる工程と、配線の上部側を覆うとともに配線の側部で第１のバリア層と重なり合って配線を第１バリア層とともに覆う第２のバリア層を形成する工程とを備えていることから、配線は第１のバリア層と第２のバリア層とにより被覆される。

【００２０】そのため、配線のストレスが第１のバリア層および第２のバリア層に加えられても、第１のバリア層と第２のバリア層とが重なり合っていることにより、たとえ、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層と第２のバリア層との接触が保たれる。すなわち、第１のバリア層と第２のバリア層とを重なり合うように形成することにより、バリア層同志の密着力が強化されている。したがって、第１のバリア層と第２のバリア層とが離れないので、その間に隙間が開いて配線を構成する金属が外部に移動（もしくは拡散）することはない。よって、配線を銅もしくは銅合金で形成したとしても、配線中の銅が絶縁膜中に移動することはない。

【００２１】第２の半導体装置の製造方法は、絶縁膜に凹部を形成した後、この凹部の内面に第１のバリア層を形成するとともに凹部の内部に導電体を埋め込むことで配線を形成する工程と、第１のバリア層の上側部近傍の絶縁膜を除去して溝を形成する工程と、配線の上部側を覆うとともに溝を埋め込む状態に第２のバリア層を形成する工程とを備えた製造方法である。

【００２２】上記第２の半導体装置の製造方法では、絶縁膜に形成した凹部の内面に第１のバリア層を形成するとともに凹部の内部に導電体を埋め込むことで配線を形成する工程と、第１のバリア層の上側部近傍の絶縁膜を除去して溝を形成する工程と、配線の上部側を覆うとともに溝を埋め込む状態に第２のバリア層を形成する工程とを備えていることから、配線は第１のバリア層と第２のバリア層とにより被覆される。

【００２３】そのため、配線のストレスが第１のバリア層および第２のバリア層に加えられても、第１のバリア層と第２のバリア層とが重なり合っていることにより、たとえ、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層と第２のバリア層との接触が保たれる。すなわち、第１のバリア層と第２のバリア層とを重なり合うように形成することにより、バリア層同志の密着力が強化されるためである。したがって、第１のバリア層と第２のバリア層とが離れないので、その間に隙間が開いて配線を構成する金属が外部に移動（もしくは拡散）することはない。よって、配線を銅もしくは銅合金で形成したとしても、配線中の銅が絶縁膜中に移動することはない。

【００２４】第３の半導体装置の製造方法は、絶縁膜に凹部を形成した後、この凹部の内面に第１のバリア層を形成するとともに凹部の内部に導電体を埋め込むことで配線を形成する工程と、絶縁膜表面よりも低くなるように配線の上部を除去する工程と、配線の上部側を覆うとともに配線の上側部で第１のバリア層と重なり合って配線を第１バリア層とともに覆う第２のバリア層を形成する工程とを備えた製造方法である。

【００２５】上記第３の半導体装置の製造方法では、絶縁膜に形成した凹部の内面に第１のバリア層を形成するとともに凹部の内部に導電体を埋め込むことで配線を形成する工程と、絶縁膜表面よりも低くなるように配線の上部を除去する工程と、配線の上部側を覆うとともに配線の上側部で第１のバリア層と重なり合って配線を第１バリア層とともに覆う第２のバリア層を形成する工程とを備えていることから、配線は第１のバリア層と第２のバリア層とにより被覆される。

【００２６】そのため、配線のストレスが第１のバリア層および第２のバリア層に加えられても、第１のバリア層と第２のバリア層とが重なり合っていることにより、たとえ、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層と第２のバリア層との接触が保たれる。すなわち、第１のバリア層と第２のバリア層とを重なり合うように形成することにより、バリア層同志の密着力が強化されるためである。したがって、第１のバリア層と第２のバリア層とが離れないので、その間に隙間が開いて配線を構成する金属が外部に移動（もしくは拡散）することはない。よって、配線を銅もしくは銅合金で形成したとしても、配線中の銅が絶縁膜中に移動することはない。

【００２７】

【発明の実施の形態】本発明の半導体装置に係わる第１の実施の形態を、図１の概略構成断面図によって説明する。

【００２８】図１に示すように、半導体装置の一部を構成する層間絶縁膜２１には凹部（以下、配線溝として説

明する）２２が形成されている。上記層間絶縁膜２１は、例えば酸化シリコンで形成されている。この配線溝２２には、第１のバリア層２３を介して配線２４が上記層間絶縁膜２１の上面より突出する状態に形成されている。このように、第１のバリア層２３は上記配線２４を下部側より被覆している。第１のバリア層２３は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化タンタルもしくはタンタルで形成されている。上記配線２４は、例えば銅もしくは銅合金で形成されている。

【００２９】さらに上記配線２４を上部側より被覆する第２のバリア層２５が、上記第１のバリア層２３と上記配線２４の側部（側面）で重なり合う状態に形成されている。この第２バリア層２５は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化シリコンで形成されている。このようにして、配線２４は第１のバリア層２３と第２のバリア層２５とによって被覆されている。

【００３０】なお、上記層間絶縁膜２１は、図示はしないが、例えば半導体基板上に形成されたトランジスタ、容量、抵抗等の半導体素子や配線を被覆するものであってもよく、または平坦化のためのものであってもよく、または配線層を被覆するものであってもよい。すなわち、通常の半導体装置に用いられている層間絶縁膜である。

【００３１】上記第１の実施の形態では、配線２４の下部側よりこの配線２４を被覆する第１のバリア層２３と、上記配線２４の上部側よりこの配線２４を被覆する第２のバリア層２５とを備え、第１のバリア層２３と第２のバリア層２５とが配線２４の側部で重なりあって配線２４が被覆されていることから、配線２４のストレスが第１のバリア層２３および第２のバリア層２５に加えられても、第１のバリア層２３と第２のバリア層２５とが重なり合っていることにより、たとえ、どちらかのバリア層（例えば第２のバリア層２５）がずれたとしても、重なりあっている部分で第１のバリア層２３と第２のバリア層２５とは接触を保持している。

【００３２】すなわち、第１のバリア層２３と第２のバリア層２５とが重なり合うことにより、バリア層同志の密着力が強化されている。そのため、第１のバリア層２３と第２のバリア層２５とが離れて、その間から配線２４を構成する金属が外部、すなわち層間絶縁膜２１の方向に移動（もしくは拡散）することがない。すなわち、配線２４のストレスが働いても、第１のバリア層２３と第２のバリア層２５とで配線２４を被覆している状態は変わらない。したがって、配線２４を構成する銅が、例えばイオン化して配線２４の周囲の層間絶縁膜２１中に移動することがない。

【００３３】次に、本発明の半導体装置に係わる第２の実施の形態を、図２の概略構成断面図によって説明する。なお、図２では、前記図１と同様の構成部品には同一符号を付与する。

【００３４】図２に示すように、半導体装置の一部を構成する層間絶縁膜２１には凹部（以下、配線溝として説明する）２２が形成されている。上記層間絶縁膜２１は、例えば酸化シリコンで形成されている。この配線溝２２には、第１のバリア層２３を介して配線２４が形成されている。このように、第１のバリア層２３は上記配線２４を下部側より被覆している。第１のバリア層２３は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化タンタルもしくはタンタルで形成されている。上記配線２４は、例えば銅もしくは銅合金で形成されている。

【００３５】さらに上記第１のバリア層２３の上側部の層間絶縁膜２１には溝２６が形成され、その溝２６を埋め込むようにかつ上記配線２４を上部側より被覆するように第２のバリア層２５が形成されている。このように第２のバリア層２５が形成されていることから、第２のバリア層２５は上記第１のバリア層２３と上記配線２４の側部（側面）で重なり合う状態になっている。この第２バリア層２５は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化シリコンで形成されている。もしくは、炭化シリコン、タンタル、タンタル合金、窒化タンタル等で形成することも可能である。このようにして、配線２４は第１のバリア層２３と第２のバリア層２５とによって被覆されている。

【００３６】上記第２の実施の形態では、配線２４の側部で第１のバリア層２３と第２のバリア層２５とが重なり合う状態に、第１のバリア層２３と第２のバリア層２５とで配線２４を被覆しているので、前記第１の実施の形態を同様に、配線２４を構成する銅が、例えばイオン化して配線２４の周囲の層間絶縁膜２１中に移動するのを、第１のバリア層２３と第２のバリア層２５とで阻止することができる。

【００３７】次に、本発明の半導体装置に係わる第３の実施の形態を、図３の概略構成断面図によって説明する。なお、図３では、前記図１と同様の構成部品には同一符号を付与する。

【００３８】図３に示すように、半導体装置の一部を構成する層間絶縁膜２１には凹部（以下、配線溝として説明する）２２が形成されている。上記層間絶縁膜２１は、例えば酸化シリコンで形成されている。この配線溝２２には、第１のバリア層２３を介して配線２４が形成されている。このように、第１のバリア層２３は上記配線２４を下部側より被覆している。第１のバリア層２３は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化タンタルもしくはタンタルで形成されている。上記配線２４は、例えば銅もしくは銅合金で形成されている。

【００３９】さらに上記第１のバリア層２３の上側部近

傍の層間絶縁膜２１には溝２６が形成され、その溝２６を埋め込むようにかつ上記配線２４を上部側より被覆するように第２のバリア層２７が形成されている。このように第２のバリア層２７が形成されていることから、第２のバリア層２７は上記第１のバリア層２３と上記配線２４の側部（側面）で重なり合う状態になっている。この第２バリア層２７は、銅原子および銅イオンに対してバリア性を有するような材料として、例えばアリールエーテルのような低誘電率有機膜で形成されている。このようにして、配線２４は第１のバリア層２３と第２のバリア層２７とによって被覆されている。

【００４０】なお、上記第２のバリア層に低誘電率有機膜を用いることができるのは、低誘電率有機膜に対する銅の拡散係数が小さいためである。

【００４１】上記第３の実施の形態では、配線２４の側部で第１のバリア層２３と第２のバリア層２７とが重なり合う状態に、第１のバリア層２３と第２のバリア層２７とで配線２４を被覆しているので、前記第１の実施の形態を同様に、配線２４を構成する銅が、例えばイオン化して配線２４の周囲の層間絶縁膜２１中に移動するのを、第１のバリア層２３と第２のバリア層２７とで阻止することができる。また、第２のバリア層２７は、配線２４とその上部に形成される配線（図示せず）との配線間の層間絶縁膜として用いることが可能である。

【００４２】次に、本発明の半導体装置に係わる第４の実施の形態を、図４の概略構成断面図によって説明する。なお、図４では、前記図１と同様の構成部品には同一符号を付与する。

【００４３】図４に示すように、半導体装置の一部を構成する層間絶縁膜２１には凹部（以下、配線溝として説明する）２２が形成されている。上記層間絶縁膜２１は、例えば酸化シリコンで形成されている。この配線溝２２の内壁（底部も含む）には、第１のバリア層２３が形成されている。上記第１のバリア層２３は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化タンタルもしくはタンタルで形成されている。さらに上記配線溝２２には、上記第１のバリア層２３を介して配線２４が上記層間絶縁膜２１の上面より凹んだ状態に形成されている。この配線２４は、例えば銅もしくは銅合金で形成されている。

【００４４】したがって、上記配線溝２２内において上記配線２４の側方上にも上記第１のバリア層２３が形成され、その第１のバリア層２３によって上記配線２４の下部側が被覆されている。

【００４５】さらに上記配線２４を上部側より被覆する第２のバリア層２５が、上記第１のバリア層２３と上記配線溝２２の側壁で重なり合う状態に形成されている。この第２バリア層２５は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化シリコンで形成されている。このようにして、配線２４は第１のバリア層２３と第２のバリア層２５とによって被覆されている。

【００４６】なお、上記層間絶縁膜２１は、図示はしないが、例えば半導体基板上に形成されたトランジスタ、容量、抵抗等の半導体素子や配線を被覆するものであってもよく、または平坦化のためのものであってもよく、または配線層を被覆するものであってもよい。すなわち、通常の半導体装置に用いられている層間絶縁膜である。

【００４７】上記第４の実施の形態では、配線２４の下部側よりこの配線２４を被覆する第１のバリア層２３と、上記配線２４の上部側よりこの配線２４を被覆する第２のバリア層２５とを備え、第１のバリア層２３と第２のバリア層２５とが配線溝２２の側部で重なりあって配線２４が被覆されていることから、配線２４のストレスが第１のバリア層２３および第２のバリア層２５に加えられても、第１のバリア層２３と第２のバリア層２５とが重なり合っていることにより、たとえ、どちらかのバリア層（例えば第２のバリア層２５）がずれたとしても、重なりあっている部分で第１のバリア層２３と第２のバリア層２５との接触は保持される。

【００４８】すなわち、第１のバリア層２３と第２のバリア層２５とが重なり合うことにより、バリア層同志の密着力が強化されている。そのため、第１のバリア層２３と第２のバリア層２５とが離れて、その間から配線２４を構成する金属が外部、すなわち層間絶縁膜２１の方向に移動（もしくは拡散）することがない。すなわち、配線２４のストレスが働いても、第１のバリア層２３と第２のバリア層２５とで配線２４を被覆している状態は変わらない。したがって、配線２４を構成する銅が、例えばイオン化して配線２４の周囲の層間絶縁膜２１中に移動することがない。

【００４９】次に、本発明の第１の製造方法に係わる実施の形態を、図５の製造工程図によって説明する。図５では、一例として、前記図１によって説明した半導体装置の製造方法を示し、前記図１で示した構成部品と同様の部品には同一符号を付与する。

【００５０】図５の（１）に示すように、半導体基板（図示省略）には、半導体素子（例えば、トランジスタ、容量、抵抗等）が形成され、さらに下層配線、配線パターン等が形成されている。そのような半導体基板上には、それらの素子、配線等を覆う絶縁膜１１が形成されている。その絶縁膜１１上に、層間絶縁膜２１を形成する。この層間絶縁膜２１は、例えばアリールエーテル等の低誘電率有機膜と酸化シリコン膜との積層膜で形成する。もしくは、フッ素樹脂膜と酸化シリコン膜との積層膜、酸化フッ素化シリコン膜、有機ＳＯＧ膜、無機ＳＯＧ膜等の、いわゆる低誘電率膜で形成する。特に、デザインルールが０．１３μｍ世代以降のデバイスでは、低誘電率膜を含むことが必要である。

【００５１】その後、一般的に知られているダマシン法によって、層間絶縁膜２１に凹部（以下、配線溝として説明する）２２を形成した後、配線溝２２の内面に第１のバリア層２３を、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化タンタルもしくはタンタルで形成する。さらに、配線溝２２の内面に第１のバリア層２３を介して銅のシード層を形成した後、電解めっき法等により、配線溝２２の内部を導電体（例えば銅）で埋め込む。その後、例えばＣＭＰにより、層間絶縁膜２１上の余分な銅および第１のバリア層２３を除去して、配線溝２２の内部に第１のバリア層２３を介して銅からなる配線２４を形成する。

【００５２】次に、図５の（２）に示すように、配線２４の周囲の層間絶縁膜２１をエッチングにより除去して、層間絶縁膜２１の表面より配線２４と第１のバリア層２３とを突出させる。したがって、第１のバリア層２３は上記配線２４を下部側より被覆している状態になっている。

【００５３】上記エッチングでは、層間絶縁膜２１が酸化シリコン膜の場合、例えば濃度が０．１％～１．０％のフッ酸水溶液、ここでは一例として０．５％のフッ酸水溶液を用いて、ウェットエッチングにより除去する。なお、０．１％未満の濃度のフッ酸水溶液を用いたウエットエッチングではエッチングレートが遅くなるために実用的ではなく、１．０％を越えるフッ酸水溶液を用いたウエットエッチングでは金属部分もエッチングされてしまうので好ましくない。また、層間絶縁膜２１が、アリールエーテルのような低誘電率有機膜の場合には、水素プラズマエッチングもしくは窒素プラズマエッチングにより除去する。なお、酸素プラズマエッチングを用いることは、配線２４の銅を酸化させ、不良の原因となるため、好ましくない。また、配線２４の酸化防止の観点から、このエッチングと次に行う第２のバリア層の形成までを非酸化性雰囲気で行うことが望ましい。すなわち、いわゆるin situ 処理を行うことが望ましい。

【００５４】また、上記層間絶縁膜２１のエッチングをフッ化炭素系のガスを用いたドライエッチングにより行うことも可能である。この場合、第１のバリア層２３の上部もエッチングされる場合がある。なお、第１のバリア層２３の上部がエッチングされたとしても、その後に形成される第２のバリア層の第１のバリア層２３に対する重なり量が十分に確保できるように、すなわち、エッチング後の層間絶縁膜２１の表面より第１のバリア層２３を３０ｎｍ以上の高さに残すように、上記エッチングを行う必要がある。

【００５５】上記層間絶縁膜２１のエッチングによって、層間絶縁膜２１と第１のバリア層２３との段差の高さを少なくとも３０ｎｍ以上に形成することが好ましい。もし、上記段差が３０ｎｍ以下の場合には、後に形成する第２のバリア層との重なり部分が少なくなり、十分なバリア性を確保することが困難になり、従来のバリア層の構造と同様になってしまうためである。

【００５６】次に、図５の（３）に示すように、上記配線２４を覆うように上記層間絶縁膜２１上に第２のバリア層２５を形成する。この第２のバリア層２５は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化シリコン、水素化シリコンカーボン等の絶縁膜で形成する。その製造方法としては、ＣＶＤ法が好ましい。その他の成膜方法としては、スパッタリング、ゾルゲル法等の成膜方法を用いることもできる。ＣＶＤ法により成膜する場合は、上記層間絶縁膜２１のエッチングとin situ 処理することが好ましい。例えば、酸化シリコン膜を希フッ酸水溶液でエッチングした後、水素プラズマを用いたエッチングにより、５ｎｍ～２０ｎｍ程度エッチングを行い、その後、連続して化学的気相成長（以下、ＣＶＤという、ＣＶＤはChemical Vapour Depositionの略）法により窒化シリコン膜からなる第２のバリア層２５を形成する。

【００５７】層間絶縁膜２１が有機膜の場合には、水素プラズマもしくは窒素プラズマを用いたエッチングにより１０ｎｍ～１００ｎｍ程度エッチングし、その後、ＣＶＤ法により第２のバリア層２５を窒化シリコン膜で形成する。このとき、窒化シリコン膜は２０ｎｍ～１００ｎｍ程度の厚さに形成することが望ましい。２０ｎｍ未満では十分なバリア性が得られない。一方、１００ｎｍを超える厚さでは、配線間容量が大きくなり、好ましくない。このように、水素プラズマを用いてエッチングすることにより、配線２４の表面の酸化膜（銅の酸化膜）をエッチングし、同時に配線２４の表面をクリーニングして、窒化シリコン膜からなる第２のバリア層２５との密着性が向上される。

【００５８】また、ＣＶＤ法で窒化シリコン膜からなる第２のバリア層２５を形成する際には、配線２４上の膜厚よりも配線２４の側壁の膜厚が薄くなるように形成することが好ましい。それは、配線間に窒化シリコン膜が形成されると、配線間容量が上昇するため、極力、配線間容量の上昇を抑制するためである。そのため、ＣＶＤ法では、方向性を有するＣＶＤ法として、高密度プラズマＣＶＤ装置を用いて成膜を行うとよい。もしくは、平行平板型プラズマＣＶＤ装置を用いて成膜を行うとよい。その成膜条件としては、ステップカバリッジが３０％程度以下となる条件とする。平行平板型プラズマＣＶＤ装置を用いた場合の成膜条件としては、一例として、成膜雰囲気の圧力を１．０３ｋＰａ、成膜温度を４００℃、プロセスガス比をモノシラン〔SiH_4〕：アンモニア（NH_3）＝３：１程度に設定する。さらに、ＣＶＤの直前に、水素プラズマおよび窒素プラズマのうちの少なくとも一方を含むプラズマ処理を行うことが好ましい。高密度プラズマＣＶＤ装置を用いた場合の成膜条件としては、一例として、成膜雰囲気の圧力を１Ｐａ以

下、成膜温度を２００℃～４００℃、プロセスガス比をモノシラン〔SiH_4〕：窒素（N_2）＝３：１．５～５程度に設定する。

【００５９】上記のようにして第２のバリア層２５を成膜すると、第２のバリア層２５は、配線２４の上部側を覆うとともに配線２４の側部で第１のバリア層２３と重なり合って、配線２４を第１バリア層２３とともに被覆する。

【００６０】その後、図５の（４）に示すように、第２のバリア層２５上に層間絶縁膜３１を形成する。層間絶縁膜３１は、低誘電率膜を含むことが望ましい。本発明では、アリールエーテルを用いたが、他に、有機ＳＯＧ、無機ＳＯＧ、フッ素樹脂、キセロゲル等を用いることも可能である。

【００６１】なお、図示はしないが、上記絶縁膜１１の所定に位置に接続孔およびその内部にプラグが形成されている。また、デュアルダマシン法により配線２４を形成する場合には、上記絶縁膜１１の所定の位置にデュアルダマシン法により接続孔を形成し、配線２４を形成する際に、接続孔内部にも配線２４を形成する導電体、例えば銅を埋め込んでプラグを形成する。

【００６２】上記図５によって説明した第１の製造方法では、配線溝２２の内部に第１のバリア層２３を介して銅よりなる配線２４を形成した後、配線２４の周囲の層間絶縁膜２１を除去して、層間絶縁膜２１の表面より配線２４と第１のバリア層２３とを突出させ、その後、配線２４の上部側を覆うとともに配線２４の側部で第１のバリア層２３と重なり合って配線２４を第１バリア層２３とともに覆う第２のバリア層２５を形成することから、配線２４は第１のバリア層２３と第２のバリア層２５とにより被覆される。

【００６３】そのため、配線２４のストレスが第１のバリア層２３および第２のバリア層２５に加えられても、第１のバリア層２３と第２のバリア層２５とが重なり合っていることにより、たとえ、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層２３と第２のバリア層２５との接触が保たれる。すなわち、第１のバリア層２３と第２のバリア層２５とを重なり合うように形成することにより、バリア層同志の密着力が強化されるためである。したがって、第１のバリア層２３と第２のバリア層２５とが離れないので、その間に隙間が開いて配線２４を構成する銅が外部に移動（もしくは拡散）することはない。よって、配線２４を上記のように銅（もしくは銅合金）で形成し、上記層間絶縁膜２１に酸化シリコン膜を用いたとしても、配線２４中の銅、例えばイオン化した銅が層間絶縁膜２１中に移動することはない。

【００６４】また、上記第１の製造方法において、層間絶縁膜２１が低誘電率有機膜と酸化シリコン膜との積層構造となっていて、層間絶縁膜２１の上部が酸化シリコン膜で形成され、その酸化シリコン膜の膜厚が３０ｎｍ～１００ｎｍ程度の場合には、配線２４および第１のバリア層２３を突出させるために層間絶縁膜２１の上部を除去する工程において、層間絶縁膜２１の酸化シリコン膜部分を全て除去してもよい。

【００６５】次に、本発明の第２の製造方法に係わる第１の実施の形態を、図６の製造工程図によって説明する。図６では、一例として、前記図２によって説明した半導体装置の製造方法を示し、前記図２で示した構成部品と同様の部品には同一符号を付与する。

【００６６】図６の（１）に示すように、前記図５の（１）によって説明したのと同様の方法、つまり一般に知られているダマシン法により、層間絶縁膜２１に凹部（以下、配線溝として説明する）２２を形成した後、配線溝２２の内面に第１のバリア層２３を、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化タンタルもしくはタンタルで形成する。さらに、配線溝２２の内面に第１のバリア層２３を介して銅のシード層を形成した後、電解めっき法等により、配線溝２２の内部を導電体（例えば銅）で埋め込む。その後、例えばＣＭＰにより、層間絶縁膜２１上の余分な銅および第１のバリア層２３を除去して、配線溝２２の内部に第１のバリア層２３を介して銅からなる配線２４を形成する。

【００６７】次いで図６の（２）に示すように、層間絶縁膜２１をエッチングする。その際のエッチング条件を、第１のバリア層２３の側周における層間絶縁膜２１がエッチングされるような条件を選択する。例えば層間絶縁膜２１が１０％～２０％の炭素を含む酸化シリコン膜の場合、マグネトロン型エッチング装置を用いて、エッチングガスにトリフルオロメタン（CHF_3）〔供給流量は例えば５ｓｃｃｍとする〕とアルゴン（Ａｒ）〔供給流量は例えば２０ｓｃｃｍとする〕と酸素（O_2）〔供給流量は例えば５ｓｃｃｍとする〕とを用い、一例として、エッチング雰囲気の圧力を５Ｐａ、印加電力を６００Ｗに設定して、層間絶縁膜２１を全面エッチバックすればよい。このような条件でエッチバックすることで、上記第１のバリア層２３の上側部近傍の層間絶縁膜２１に溝２６を形成する。

【００６８】その後、図６の（３）に示すように、上記溝２６を埋め込むようにかつ上記配線２４を上部側より被覆するように第２のバリア層２５を形成する。このように第２のバリア層２５を形成することから、第２のバリア層２５は上記第１のバリア層２３と上記配線２４の側部（側面）で重なり合う状態になる。この第２バリア層２５は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化シリコンで形成する。このようにして、配線２４は第１のバリア層２３と第２のバリア層２５とによって被覆される。

【００６９】上記図６によって説明した第２の製造方法

に係わる第１の実施の形態では、層間絶縁膜２１に形成した配線溝２２の内部に第１のバリア層２３を介して配線２４を形成し、次いで第１のバリア層２３の上側部近傍の層間絶縁膜２１を除去して溝２６を形成した後、配線２４の上部側を覆うとともに溝２６を埋め込む状態に第２のバリア層２５を形成することから、配線２４は第１のバリア層２３と第２のバリア層２５とにより被覆される。

【００７０】そのため、配線２４のストレスが第１のバリア層２３および第２のバリア層２５に加えられても、第１のバリア層２３と第２のバリア層２５とが重なり合っていることにより、たとえ、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層２３と第２のバリア層２５との接触が保たれる。すなわち、第１のバリア層２３と第２のバリア層２５とを重なり合うように形成することにより、バリア層同志の密着力が強化されるためである。したがって、第１のバリア層２３と第２のバリア層２５とが離れないので、その間に隙間が開いて配線２４を構成する銅が外部に移動（もしくは拡散）することはない。よって、配線２４を上記のように銅（もしくは銅合金）で形成し、上記層間絶縁膜２１に酸化シリコン膜を用いたとしても、配線２４中の銅、例えばイオン化した銅が層間絶縁膜２１中に移動することはない。

【００７１】次に、本発明の第２の製造方法に係わる第２の実施の形態を、図７の製造工程図によって説明する。図７では、一例として、前記図３によって説明した半導体装置の製造方法を示し、前記図３で示した構成部品と同様の部品には同一符号を付与する。

【００７２】前記図６の（１）、（２）によって説明したのと同様の方法により、層間絶縁膜２１に凹部（以下、配線溝として説明する）２２を形成し、その配線溝２２の内部に第１のバリア層２３を介して銅からなる配線２４を形成する。次いで層間絶縁膜２１をエッチバックして、上記第１のバリア層２３の上側部の層間絶縁膜２１に溝２６を形成する。

【００７３】その後、図７に示すように、上記溝２６を埋め込むようにかつ上記配線２４を上部側より被覆するようにして、層間絶縁膜２１上に第２のバリア層２７を形成する。この第２バリア層２７は、銅原子および銅イオンに対してバリア性を有するような材料として、例えばアリールエーテルのような低誘電率有機膜で形成する。このようにして、第２のバリア層２７は上記第１のバリア層２３と上記配線２４の側部（側面）で重なり合う状態に形成される。

【００７４】よって、上記第１の実施の形態と同様の作用効果が得られる。すなわち、よって、配線２４を上記のように銅（もしくは銅合金）で形成し、上記層間絶縁膜２１に酸化シリコン膜を用いたとしても、第１のバリア層２３と第２のバリア層１７とで配線２４が被覆されているので、配線２４中の銅、例えばイオン化した銅が層間絶縁膜２１中に移動することはない。

【００７５】次に、本発明の第３の製造方法に係わる実施の形態を、図８の製造工程図によって説明する。図８では、一例として、前記図４によって説明した半導体装置の製造方法を示し、前記図４で示した構成部品と同様の部品には同一符号を付与する。

【００７６】図８の（１）に示すように、半導体基板（図示省略）には、半導体素子（例えば、トランジスタ、容量、抵抗等）が形成され、さらに下層配線、配線パターン等が形成されている。そのような半導体基板上には、それらの素子、配線等を覆う絶縁膜１１が形成されている。その絶縁膜１１上に、層間絶縁膜２１を形成する。この層間絶縁膜２１は、例えばアリールエーテル等の有機膜と酸化シリコン膜との積層膜で形成する。もしくは、フッ素樹脂膜と酸化シリコン膜との積層膜、酸化フッ素化シリコン膜、有機ＳＯＧ膜、無機ＳＯＧ膜等の、いわゆる低誘電率膜で形成する。特に、デザインルールが０．１３μｍ世代以降のデバイスでは、低誘電率膜を含むことが必要である。

【００７７】その後、一般的に知られているダマシン法によって、層間絶縁膜２１に凹部（以下溝として説明する）を形成した後、配線溝２２の内面に第１のバリア層２３を、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化タンタルもしくはタンタルで形成する。さらに、配線溝２２の内面に第１のバリア層２３を介して銅のシード層を形成した後、電解めっき法等により、配線溝２２の内部を導電体（例えば銅）で埋め込む。その後、例えばＣＭＰにより、層間絶縁膜２１上の余分な銅および第１のバリア層２３を除去して、配線溝２２の内部に第１のバリア層２３を介して銅からなる配線２４を形成する。

【００７８】次に、図８の（２）に示すように、層間絶縁膜２１の表面よりも配線２４の上面が低くなるいように配線２４の上部のみを選択的にエッチングする。上記エッチングによって、配線２４と第１のバリア層２３との段差の高さを少なくとも３０ｎｍ以上に形成することが好ましい。もし、上記段差が３０ｎｍ以下の場合には、後に形成する第２のバリア層との重なり部分が少なくなり、十分なバリア性を確保することが困難になり、従来のバリア層の構造と同様になってしまうためである。

【００７９】次いで、図８の（３）に示すように、配線２４の表面を例えばスパッタエッチングもしくは水素プラズマエッチングにより、酸化膜等を除去する。続いて、例えばスパッタリングにより、配線２４を被覆するように層間絶縁膜２１上に第２のバリア層２５を形成する。上記第２のバリア層２５は、銅原子および銅イオンに対してバリア性を有するような材料として、例えばタンタル、窒化タンタル等で形成する。その他の成膜方法

としては、蒸気法、ＣＶＤ法等の成膜方法を用いることも可能である。

【００８０】なお、配線２４の表面に酸化膜を生成させないために、上記スパッタエッチングもしくは水素プラズマエッチングから第２のバリア層２５を形成するまでを非酸化性雰囲気で行うことが望ましい。例えば、いわゆるin situ 処理を行うことが望ましい。例えばスパッタエッチングにより、５ｎｍ～２０ｎｍ程度エッチングを行い、その後、連続してスパッタリングによりタンタル膜からなる第２のバリア層２５を形成する。このタンタル膜は２０ｎｍ～７５ｎｍ程度の厚さに形成することが望ましい。２０ｎｍ未満では十分なバリア性が得られない。一方、７５ｎｍを超える厚さでは、加工に時間を要し、配線抵抗が大きくなり過ぎることになる。

【００８１】その後、図８の（４）に示すように、例えばＣＭＰによって、層間絶縁膜２１上の第２のバリア層２５を除去する。この結果、配線溝２２内に第１のバリア層２３と第２のバリア層２５とが、配線２４の上側部で重なり合って、配線２４を第１バリア層２３と第２のバリア層２５とで被覆する構成が完成する。このように層間絶縁膜２１上の第２のバリア層２５を除去することから、第２のバリア層２５を導電体の窒化タンタルやタンタルで形成することが可能になる。

【００８２】その後、図示はしないが、前記第１の製造方法と同様に、第２のバリア層２５および層間絶縁膜２１上に層間絶縁膜３１を形成する。層間絶縁膜３１は、低誘電率膜を含むことが望ましい。本発明では、アリールエーテルを用いたが、他に、有機ＳＯＧ、無機ＳＯＧ、フッ素樹脂、キセロゲル等を用いることも可能である。

【００８３】なお、上記第２のバリア層２５を、前記第１の製造方法で説明した窒化シリコン膜、水素化シリコンカーボン等の絶縁膜で形成することも可能である。その場合の成膜方法、成膜条件等は、第１の製造方法で説明したのと同様である。

【００８４】また、上記第３の製造方法において、図示はしないが、上記絶縁膜１１の所定に位置に接続孔およびその内部にプラグが形成されている。また、デュアルダマシン法により配線２４を形成する場合には、上記絶縁膜１１の所定の位置にデュアルダマシン法により接続孔を形成し、配線２４を形成する際に、接続孔内部にも配線２４を形成する導電体、例えば銅を埋め込んでプラグを形成する。

【００８５】上記図８によって説明した第２の製造方法では、配線溝２２の内部に第１のバリア層２３を介して銅よりなる配線２４を形成した後、配線２４の上部を除去して、層間絶縁膜２１の表面より配線２４の上面を低くし、その後、配線２４の上部側を覆うとともに配線２４の側部で第１のバリア層２３と重なり合って配線２４を第１バリア層２３とともに覆う第２のバリア層２５を形成することから、配線２４は第１のバリア層２３と第２のバリア層２５とにより被覆されるようになる。

【００８６】そのため、配線２４のストレスが第１のバリア層２３および第２のバリア層２５に加えられても、第１のバリア層２３と第２のバリア層２５とが重なり合っていることにより、たとえ、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層２３と第２のバリア層２５との接触が保たれる。すなわち、第１のバリア層２３と第２のバリア層２５とを重なり合うように形成することにより、バリア層同志の密着力が強化されるためである。したがって、第１のバリア層２３と第２のバリア層２５とが離れないので、その間に隙間が開いて配線２４を構成する銅が外部に移動（もしくは拡散）することはない。よって、配線２４を上記のように銅（もしくは銅合金）で形成し、上記層間絶縁膜２１に酸化シリコン膜を用いたとしても、配線２４中の銅、例えばイオン化した銅が層間絶縁膜２１中に移動することはない。

【００８７】なお、本発明の半導体装置に係わる第５の実施の形態として、図９に示すような構造とすることも可能である。それを以下に説明する。

【００８８】図９に示すように、半導体装置の一部を構成する層間絶縁膜２１には凹部（以下、配線溝として説明する）２２が形成されている。この配線溝２２には、第１のバリア層２３を介して配線２４が上記層間絶縁膜２１の上面より突出する状態に形成されている。しかも第１のバリア層２３は、配線溝２２の周囲の層間絶縁膜２１上にも形成されている。このように形成するには、ＣＭＰで第１のバリア層２３上に堆積されている配線を形成するための導電体（例えば銅）を除去した後、いわゆるマスク工程（リソグラフィー技術とエッチング）により、第１のバリア層２３をパターニングする必要がある。なお、上記第１のバリア層２３は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化タンタルもしくはタンタルで形成されている。上記配線２４は、例えば銅もしくは銅合金で形成されている。

【００８９】さらに上記配線２４を上部側より被覆する第２のバリア層２５が、上記第１のバリア層２３と上記配線２４の側部（側面）で重なり合う状態に形成されている。この第２バリア層２５は、銅原子および銅イオンに対してバリア性を有するような材料として、例えば窒化シリコンで形成されている。このようにして、配線２４は第１のバリア層２３と第２のバリア層２５とによって被覆されている。

【００９０】上記第５の実施の形態でも、前記説明した第１の実施形態と同様の効果が得られる。

【００９１】上記各実施の形態で説明した第１のバリア層２３と第２のバリア層２５もしくは第２のバリア層２７との配線断面の縦方向における重なり幅は、第１のバ

リア層２３の配線２４の側面もしくは配線溝２２の側面での厚さと同程度以上が必要である、ただし、最大４５ｎｍ程度あれば十分であることは、発明者の実験により確認した。

【００９２】上記各実施の形態で説明した第１のバリア層２３および第２のバリア層２５もしくは第２のバリア層２７は、デュアルダマシン構造にも適用することが可能である。

【００９３】また、上記各実施の形態で説明した構成を上下逆にした構成であっても、本発明の範疇に入る。

【００９４】

【発明の効果】以上、説明したように本発明の半導体装置によれば、第１のバリア層により配線の下部が被覆され、第２のバリア層により配線の上部側が被覆され、第１のバリア層と第２のバリア層とが重なりあっているので、配線のストレスが第１のバリア層および第２のバリア層に加えられて、たとえ、どちらかのバリア層がずれたとしても、第１のバリア層と第２のバリア層とが離間することはなく、常に第１のバリア層と第２のバリア層とで配線を被覆することができる。そのため、配線が銅もしくは銅合金で形成されていても、配線中の銅が配線外に移動することができない。よって、配線間のショートの発生、リーク電流の発生を抑えることができ、配線信頼性の高いものとなる。

【００９５】本発明に係わる第１の半導体装置の製造方法によれば、絶縁膜に形成した凹部に導電体を埋め込むことで形成した配線の周囲の絶縁膜を除去して、絶縁膜表面より配線と第１のバリア層とを突出させた後、配線の上部側を覆うとともに配線の側部で第１のバリア層と重なり合って配線を第１バリア層とともに覆う第２のバリア層を形成するので、第１のバリア層と第２のバリア層とにより配線を完全に被覆することができる。そのため、配線のストレスが第１のバリア層および第２のバリア層に加えられて、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層と第２のバリア層との接触を保つことができるので、配線を銅もしくは銅合金で形成したとしても、配線中の銅の移動を阻止することができる。よって、配線間のショートの発生、リーク電流の発生を抑えた、配線信頼性の高いものを製造することができる。

【００９６】本発明に係わる第２の半導体装置の製造方法によれば、絶縁膜に形成した凹部内の第１のバリア層の上側部近傍の絶縁膜を除去して溝を形成した後、配線の上部側を覆いかつ溝を埋め込み、配線の側部で第１のバリア層と重なり合って配線を第１バリア層とともに覆う第２のバリア層を形成するので、第１のバリア層と第２のバリア層とにより配線を完全に被覆することができる。そのため、配線のストレスが第１のバリア層および第２のバリア層に加えられて、どちらかのバリア層がずれたとしても、重なり合っている部分で第１のバリア層と第２のバリア層との接触を保つことができるので、配線を銅もしくは銅合金で形成したとしても、配線中の銅の移動を阻止することができる。よって、配線間のショートの発生、リーク電流の発生を抑えた、配線信頼性の高いものを製造することができる。

【００９７】本発明に係わる第３の半導体装置の製造方法によれば、絶縁膜に形成した凹部導電体を埋め込むことで形成した配線の上部を除去して、絶縁膜表面より低く形成した後、配線の上部側を覆うとともに配線の上側部で第１のバリア層と重なり合って配線を第１バリア層とともに覆う第２のバリア層を形成するので、第１のバリア層と第２のバリア層とにより配線を完全に被覆することができる。そのため、上記第１の製造方法と同様に、配線を銅もしくは銅合金で形成したとしても、配線中の銅、例えばイオン化した銅の移動を阻止することができる。よって、配線間のショートの発生、リーク電流の発生を抑えた、配線信頼性の高いものを製造することができる。

【図面の簡単な説明】

【図１】本発明の半導体装置に係わる第１の実施の形態を示す概略構成断面図である。

【図２】本発明の半導体装置に係わる第２の実施の形態を示す概略構成断面図である。

【図３】本発明の半導体装置に係わる第３の実施の形態を示す概略構成断面図である。

【図４】本発明の半導体装置に係わる第４の実施の形態を示す概略構成断面図である。

【図５】本発明の第１の製造方法に係わる実施の形態を示す製造工程図である。

【図６】本発明の第２の製造方法に係わる第１の実施の形態を示す製造工程図である。

【図７】本発明の第２の製造方法に係わる第２の実施の形態を示す製造工程図である。

【図８】本発明の第３の製造方法に係わる実施の形態を示す製造工程図である。

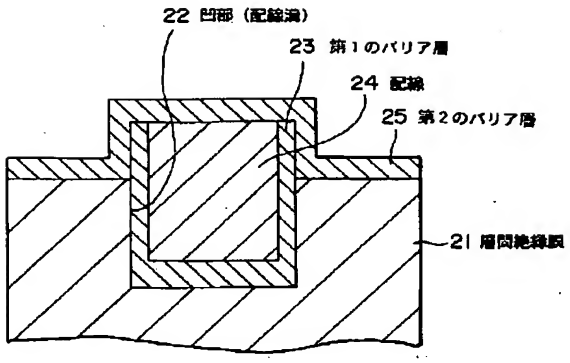
【図９】本発明の半導体装置に係わる第５の実施の形態を示す概略構成断面図である。

【図１０】従来のダマシン法による配線の形成方法を説明する製造工程図である。

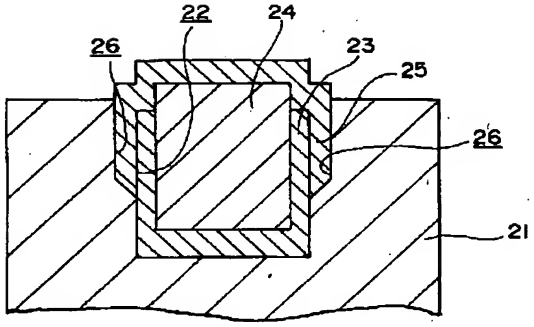
【符号の説明】

２１…層間絶縁膜、２２…凹部（配線溝）、２３…第１のバリア層、２４…配線、２５…第２のバリア層

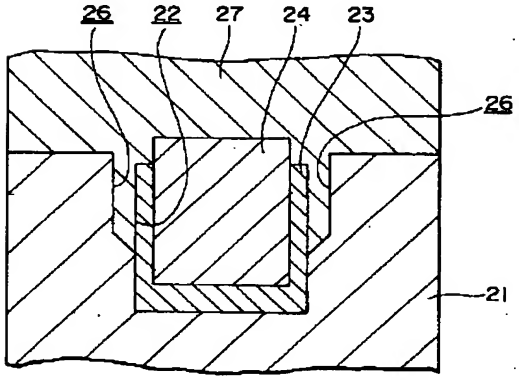
【図１】



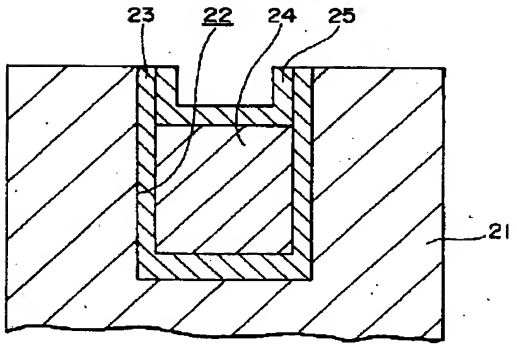
【図２】



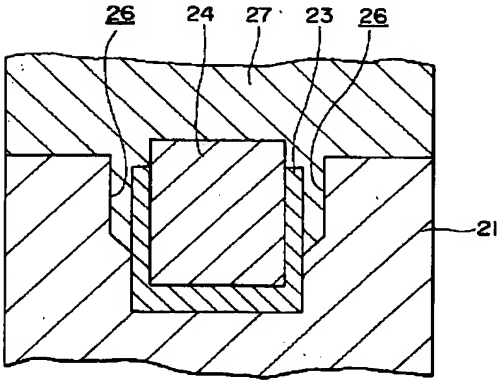
【図３】



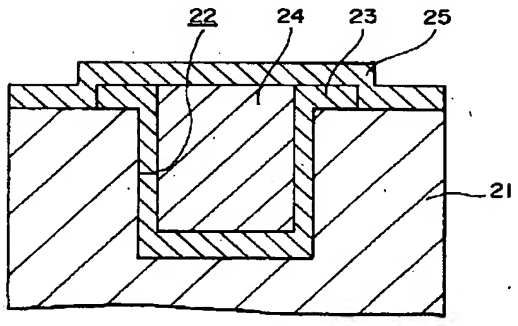
【図４】



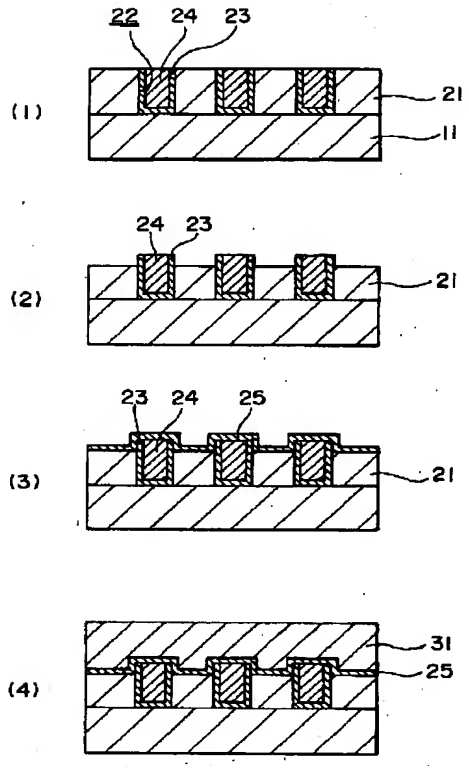
【図７】



【図９】



【図５】


(1)
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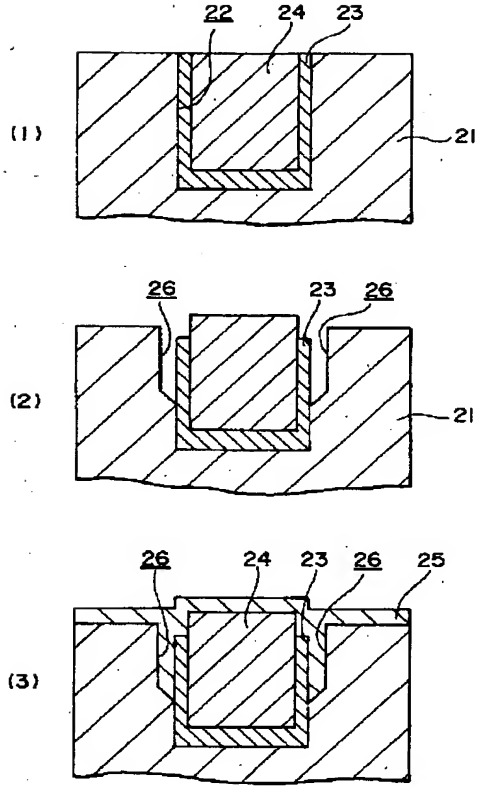
【図６】


(1)
22
24
23
21
(2)
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26
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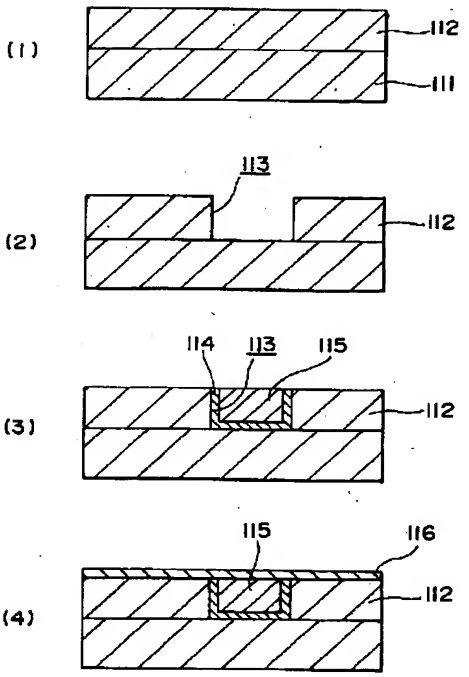
【図１０】


(1)
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111
(2)
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114
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115
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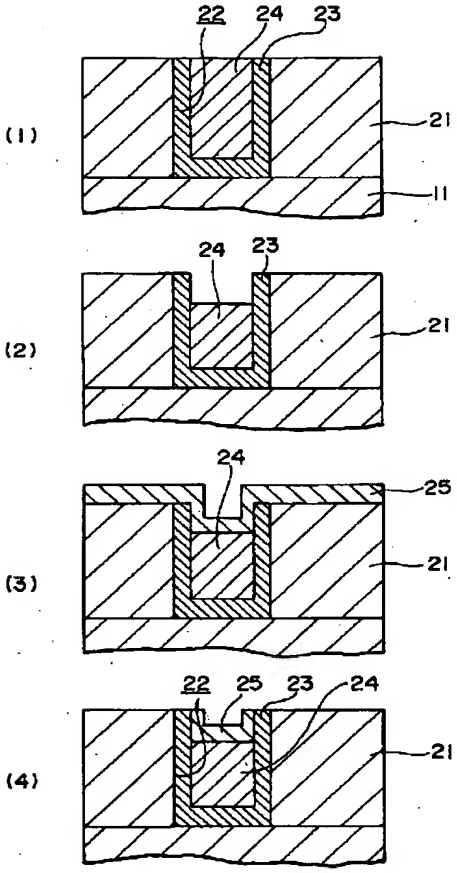
【図８】



フロントページの続き

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